ESD Basic and Circuit Design

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Outline

- Introduction
- Fundamental ESD Concept
- Brief ESD Device Design
- Brief ESD Circuit Design
- Process Effect on ESD
- ESD Test Methodologies
- ESD Failure Analysis
- Conclusions

Introduction

What's ESD ?

- Electrostatic Discharge
- Big energies occurring in a short time

What's EOS?

- Electrical Overstress
- Small energies occurring in a long time

Mainly Reference: "Review for ESD" in 2005 MCU Annual Celebration Invited Paper

All data from published papers or common ideas

What's ESD

ESD "must" conditions

- There are ESD charges.
- There are ESD voltage differences.

What's ESD

Hand carrying IC for ESD example

What's ESD

If there is only ESD zapping (no ground pin), will ESD events occur?

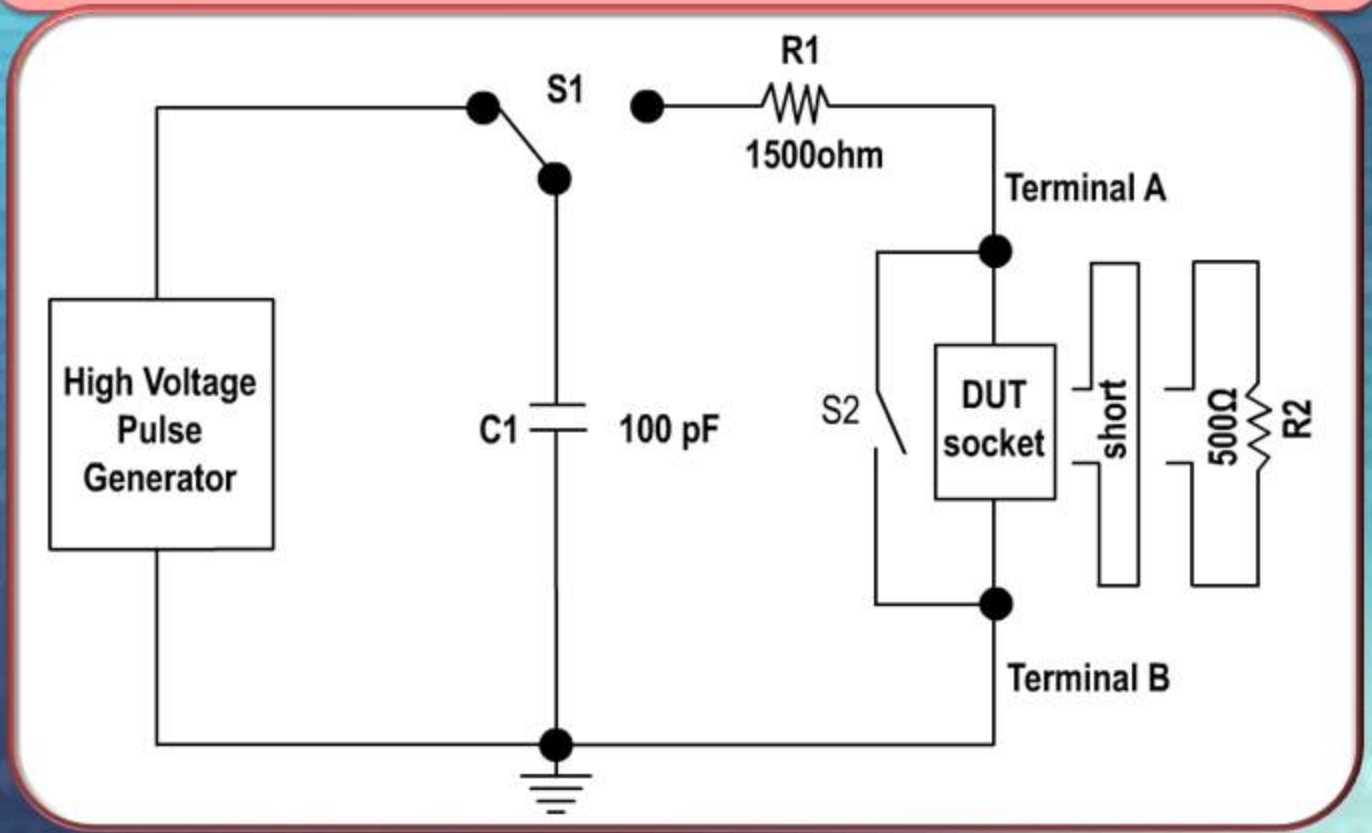
What's ESD

Does an ESD event occur at the same touched hand?

Fundamental ESD Concept: HBM (Human Body Model)

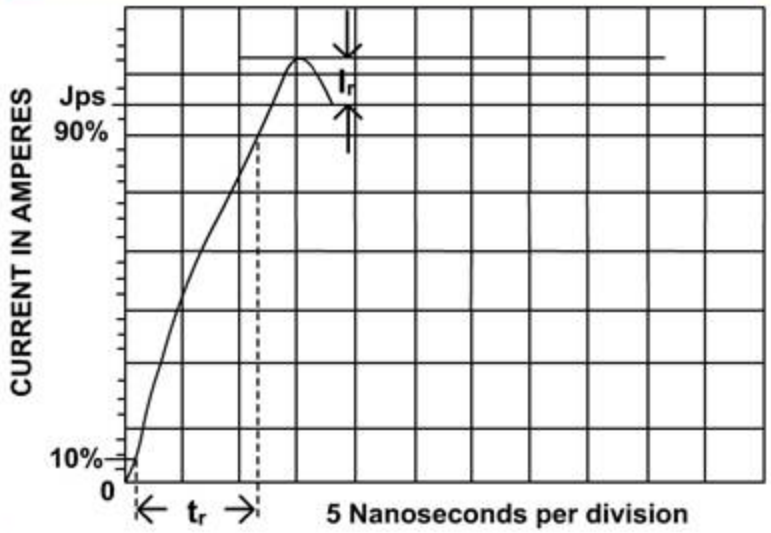
Main components for the typical equivalent HBM ESD circuit

- 1.5k ohm
- 100pf

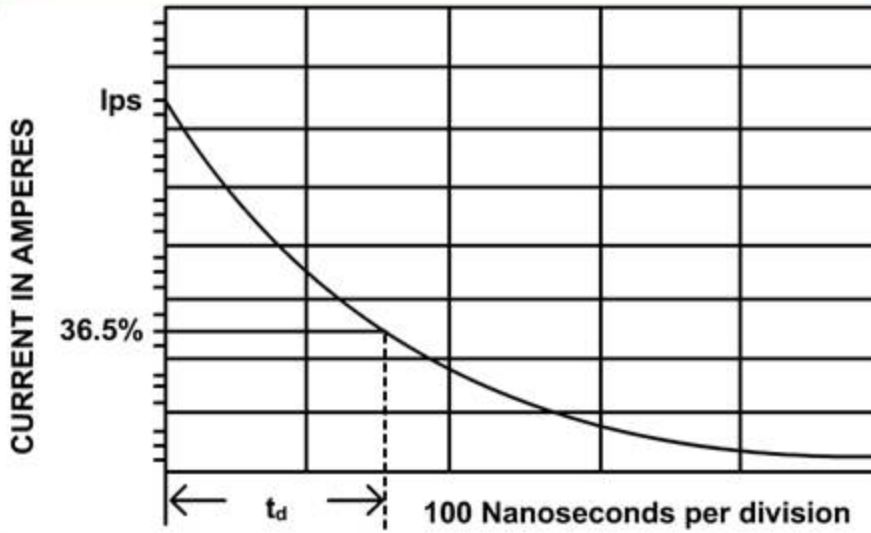


HBM waveforms

$I = I_o \exp(-t/RC)$

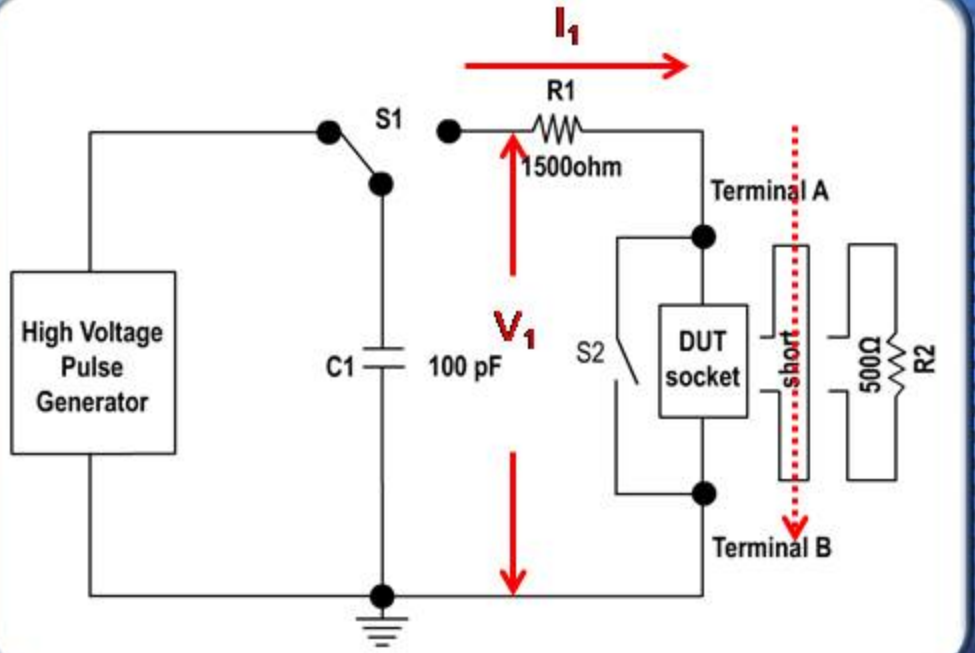


Current waveforms through a shorting wire
(a) Pulse rise time, (tr)



Current waveforms through a shorting wire
(b) Pulse decay time, (td)

The derivative



$$V_1 = I_1 * R_1$$

$$I_1 = -C_1 \frac{dV_1}{dt} = -C_1 R_1 \frac{dI_1}{dt}$$

$$\frac{dI_1}{I_1} = -\frac{dt}{C_1 R_1} \Rightarrow \int \frac{dI_1}{I_1} = \int -\frac{dt}{C_1 R_1}$$

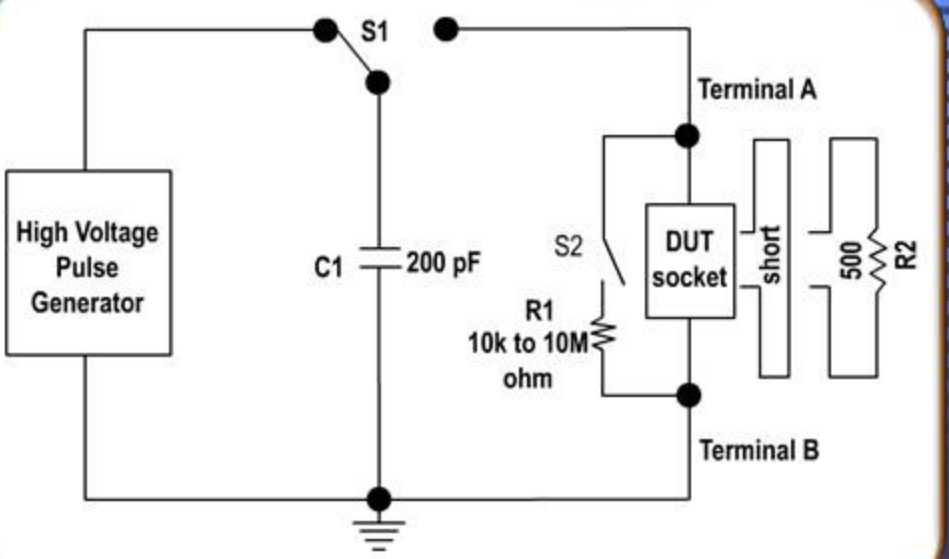
$$\ln(I_1) = A - \frac{t}{C_1 R_1} \quad (A..is..a..\text{constant})$$

$$I_1 = I_0 e^{\frac{-t}{C_1 R_1}} \Rightarrow I_0 = \frac{V_{HBM}}{R_1}$$

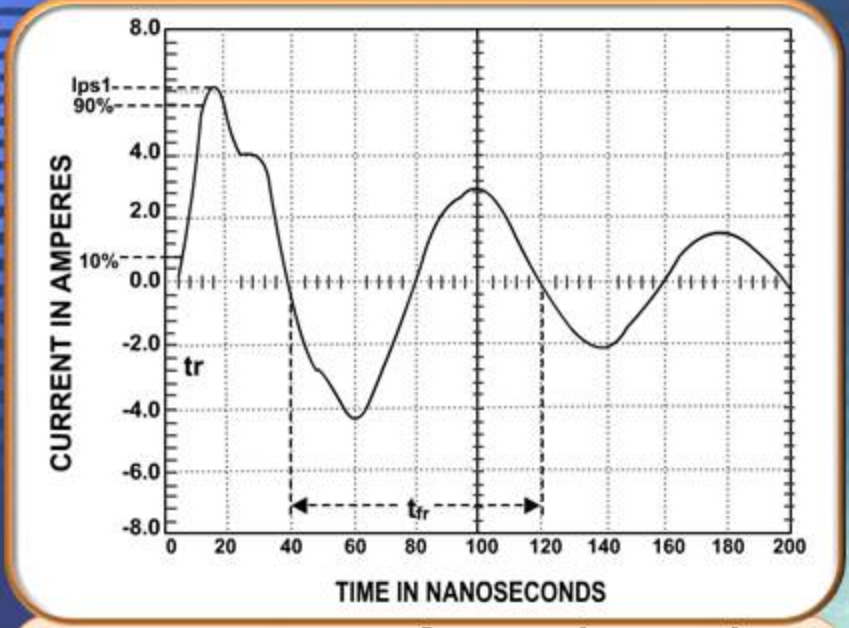
MM (Machine model)

No resistance (oscillated waveforms)

Main component: 200pf

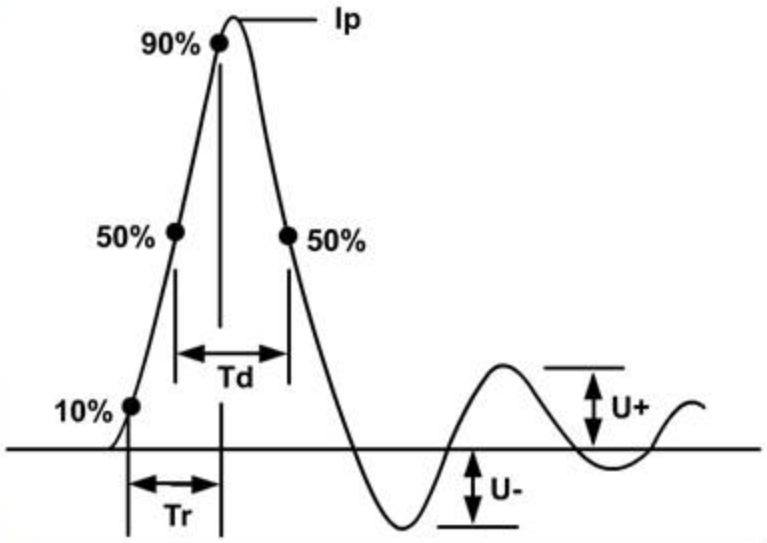


Typical equivalent MM ESD circuit



Current Waveform through a shorting wire, 400 volt discharge

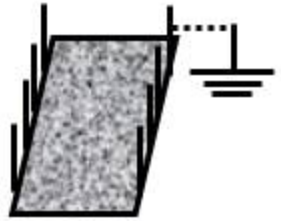
CDM (Charge device model)



CDM current waveform

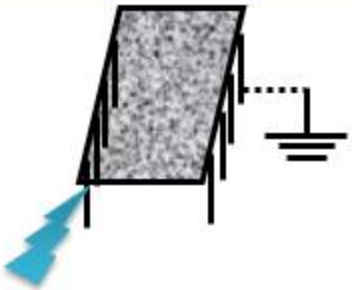
Field Induced CDM

Charge storage inside IC (P-well or n-well) from IC process, IC transportations and etc.



Charge discharge

Socket CDM

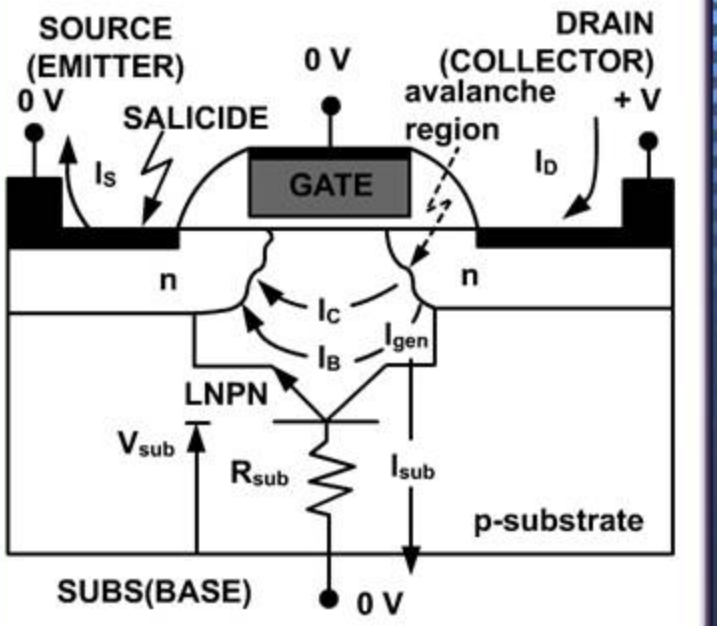


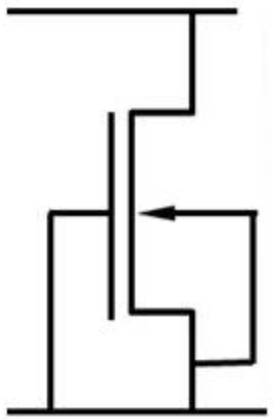
- IC is charged and discharged from IC PINs.
- IC is charged at first and then discharged.

Brief ESD Device Design

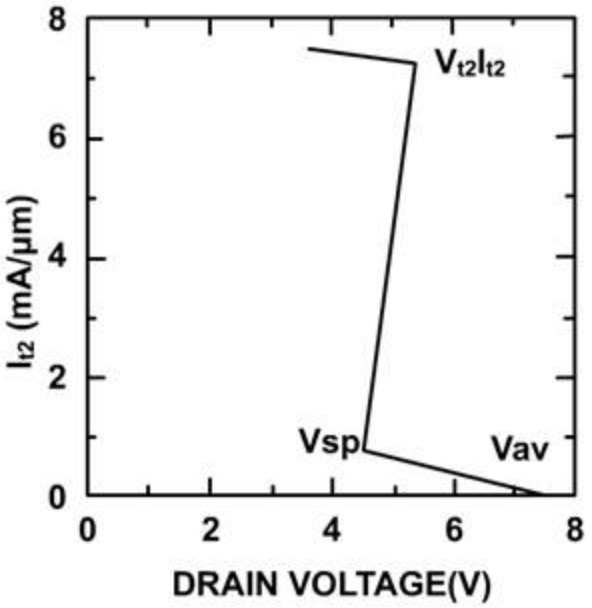
Device Characteristics

- Vav (Vt1): trigger on voltage
- Vsp : snapback voltage
- It2: secondary breakdown current
- Vt2: secondary breakdown voltage





Gate-grounded
NMOS (GGN)



ESD Guideline

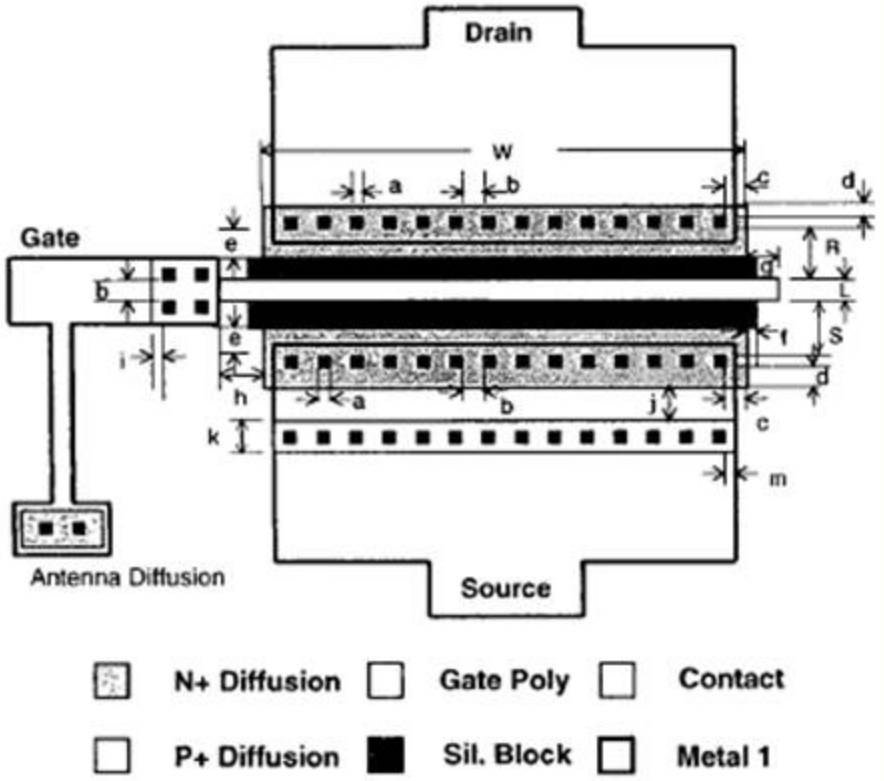


Figure 2. Single finger NMOS transistor

Dimension Definition

Table 2. Layout parameters for single finger NMOS transistors

Var.	Description of Layout Variables	Value
a	contact width	mdr
b	contact to contact spacing	mdr
c	contact to lateral side of n+ diffusion edge	3 x mdr
d	n+ contact to back side of n+ diffusion edge	mdr
e	n+ contact to salicide block spacing	mdr
f	salicide block extension outside diffusion	mdr
g	poly end overlap onto field or overhang	2 x mdr
h	poly contact pad to diffusion spacing	2 x mdr
i	contact to edge of poly contact pad	mdr
j	p+ to n+ diffusion spacing	mdr epi, 2µm bulk
k	p+ substrate tie height	mdr to cover contacts
L	poly gate length	Table 3
m	M1 to contact overhang	mdr
R	drain contact to poly spacing	Table 3
S	source contact to poly spacing	Table 3
W	n+ diffusion width	Table 3

Notes:

1. M1 width must be at least 25 µm.

2. Polysilicon finger should be contacted only on one side.

3. Polysilicon contact area has contacts.

4. Polysilicon gate tie-down is 2 µm by 1 µm rectangle with two contacts.

ESD Guideline

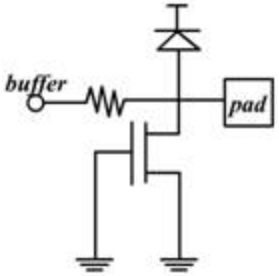
Default poly gate width size: 25µm

Table3. Layout variables for single finger NFET or NMOS transistors

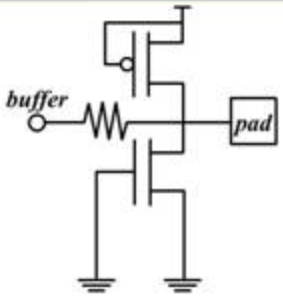
Name	W(µm)	L	R	S
NFET_1	25	mdr	mdr	mdr
NFET_1A	25	1.2 x mdr	mdr	mdr
NFET_1B	25	1.5 x mdr	mdr	mdr
NFET_1C	25	mdr	1µm	1µm
NFET_1D	25	mdr	3µm	3µm
NFET_1E	25	mdr	5µm	5µm
NFET_2	50	mdr	mdr	mdr
NFET_3	50	mdr	3µm	1µm
NFET_4	75	mdr	mdr	mdr

ESD protection structures

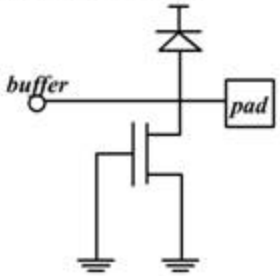
(without triggering circuits)



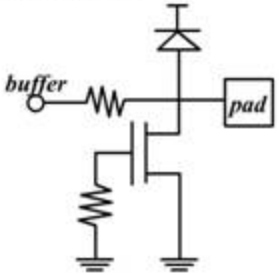
a. Grounded gate NMOS with p+N-diode



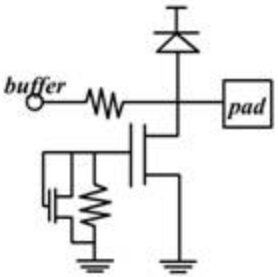
b. Grounded gate NMOS and PMOS



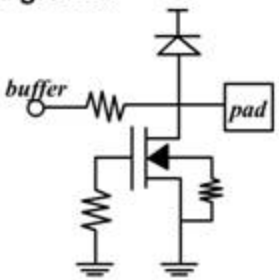
c. No buffering resistor.



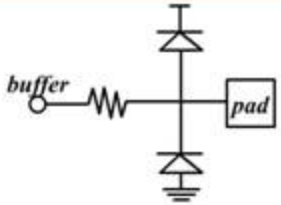
d. NMOS with gate resistor to ground.



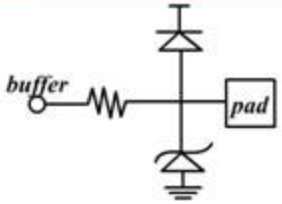
e. Clipping the NMOS gate at V_T.



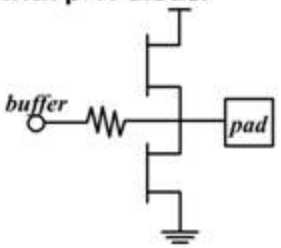
f. Enhancing the NMOS bulk resistance.



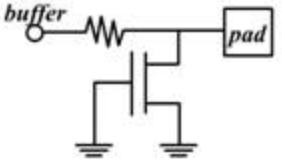
g. n+P - substrate diode with p+N-diode.



h. p+/N_{LDD} zener diode.



i. Thick-field transistors.



j. No device from pad to V_{DD}.

Used devices:

- NMOS
- PMOS
- Diode
- Zenor-diode
- Resistor
- Bipolar
- Simple gate-driven

Multiple Poly Fingers

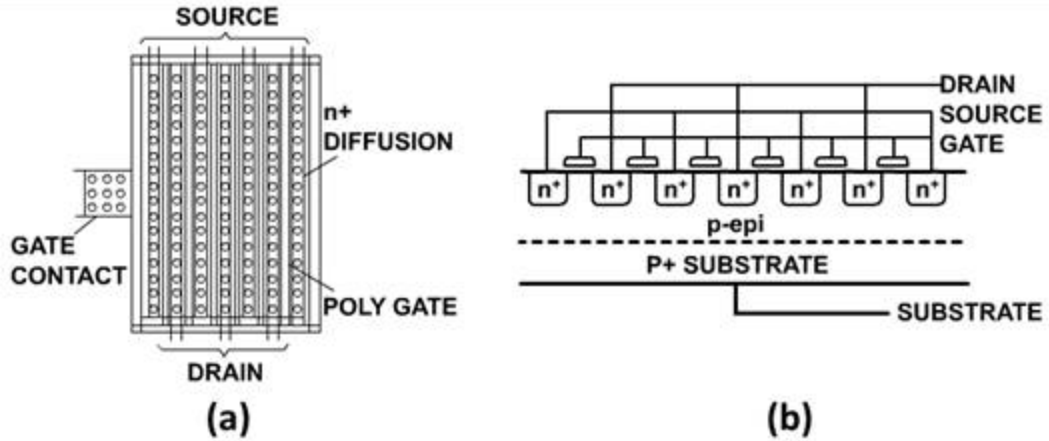


Fig.6. The layout and cross section of the ladder-structure n-MOS device for a device with 6 poly fingers each 32µm wide.

Layout type: multiple poly fingers, 32µm x6

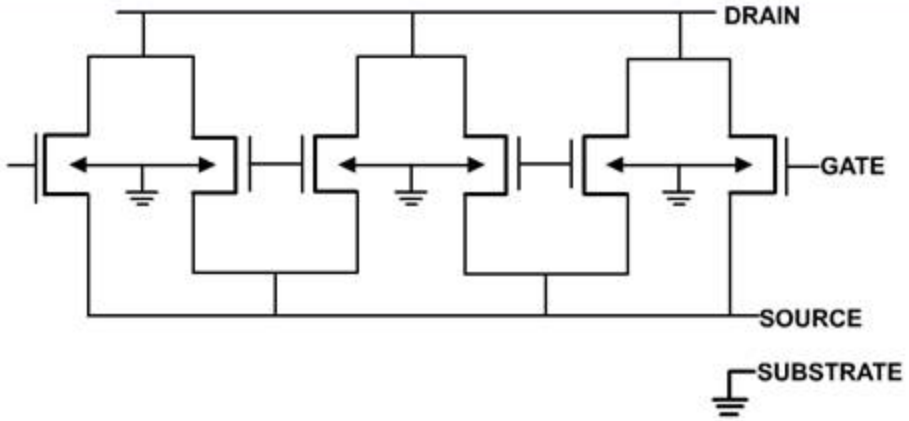


Fig.7. Equivalent circuit of the ladder-structure n-MOS device shown in Fig.6.

Circuit type: ladder-structure

Brief ESD Circuit Design

ESD Circuit Design

Top principles to design ESD circuits are as the below :

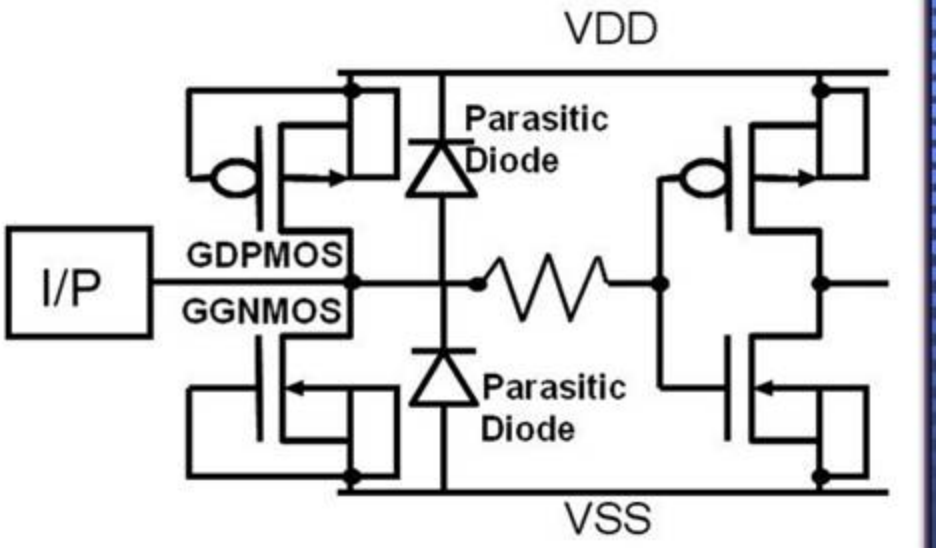
- Pass normal I/O signals and remain inactive during normal IC's operations.
- Provide CMOS integrated circuits with efficient discharging paths to bypass any ESD stress.
- Small layout area (as small as possible).
- Latch-up immunity.
- Fabrication compatible (without extra layers).

ESD Design Concerns

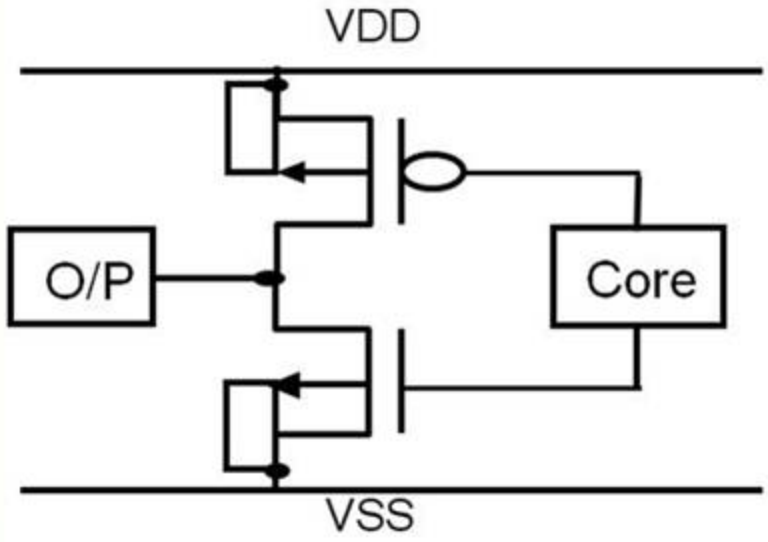
- ESD protection device/ circuit
- ESD being protected device/ circuit (Cascade NMOS and Schmitt-trigger circuit)

Four kinds of basic I/O circuit

Typical IP(input) Circuit (GGNMOS: gate grounded NMOS, GDPMOS: gate drained PMOS)



Typical input circuit: only as the input circuit, without driving output circuit



Typical output circuit

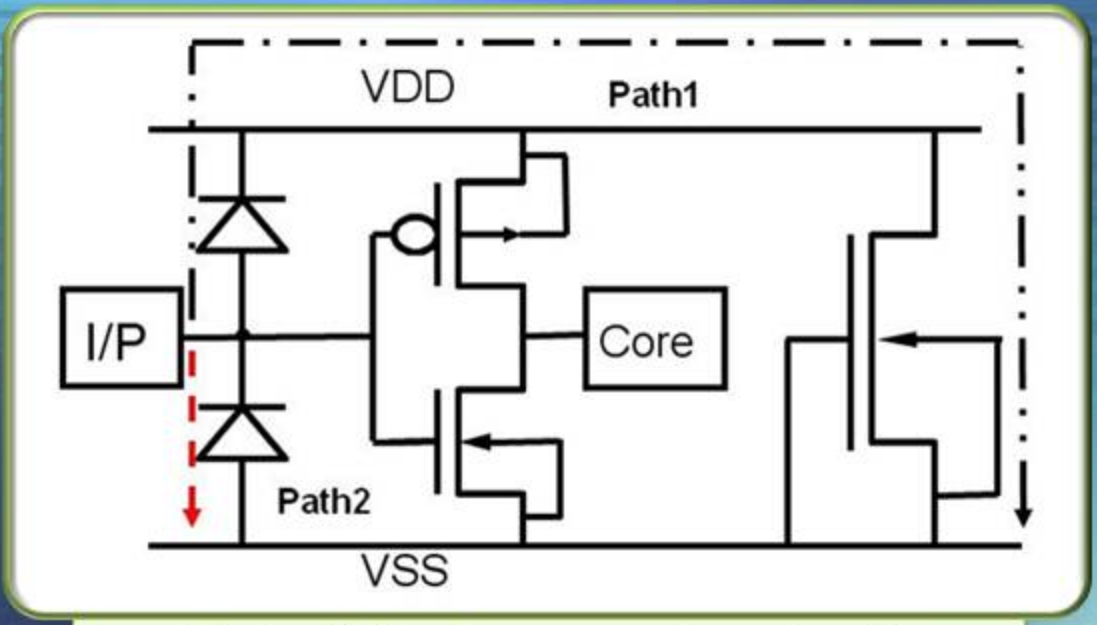
Four kinds of basic circuit: Diode

Advantages:

- Easy Layout
- Very good forward ESD currents bypass

Disadvantages:

- Only one-way ESD protection
- Bad diode string turn on voltages due to Darlington effect
- Only input circuits without driving capabilities



Typical diode protection circuit

Four kinds of basic circuit: HVT

HVT (High Voltage Tolerant) Circuit ESD Characteristics:

- Large turn on voltage
- Need extra process
- Need large layout area

HVT IO Circuit

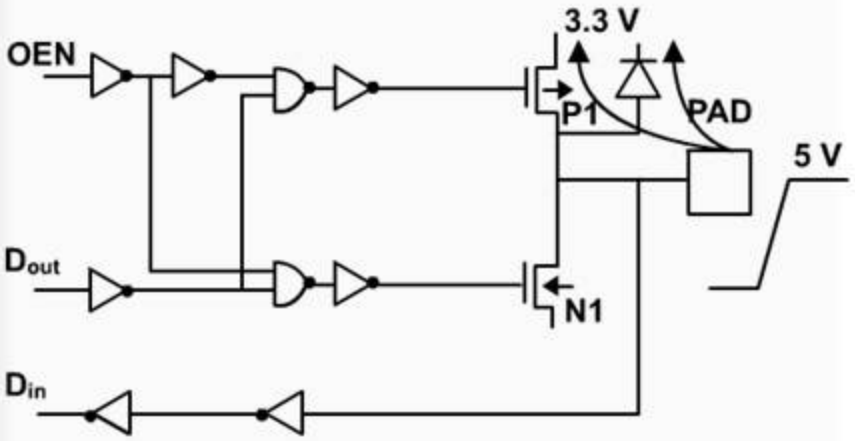


Fig. 1. Normal 3.3-V I/O buffer driven by a 5-V signal.

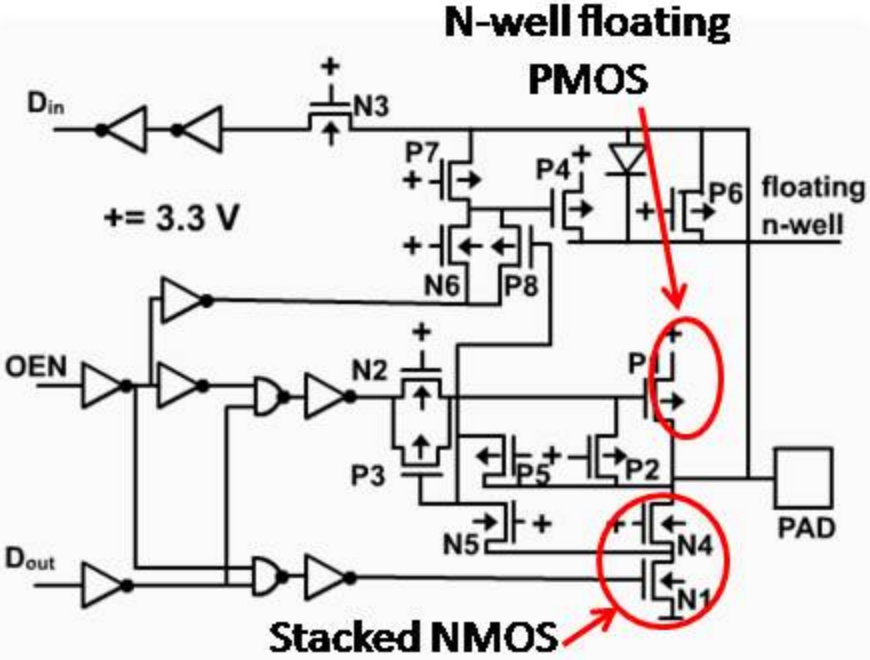


Fig. 2. Schematic representation of the I/O buffer. All drawn PMOST's P_1 to P_8 are in the floating n-well.

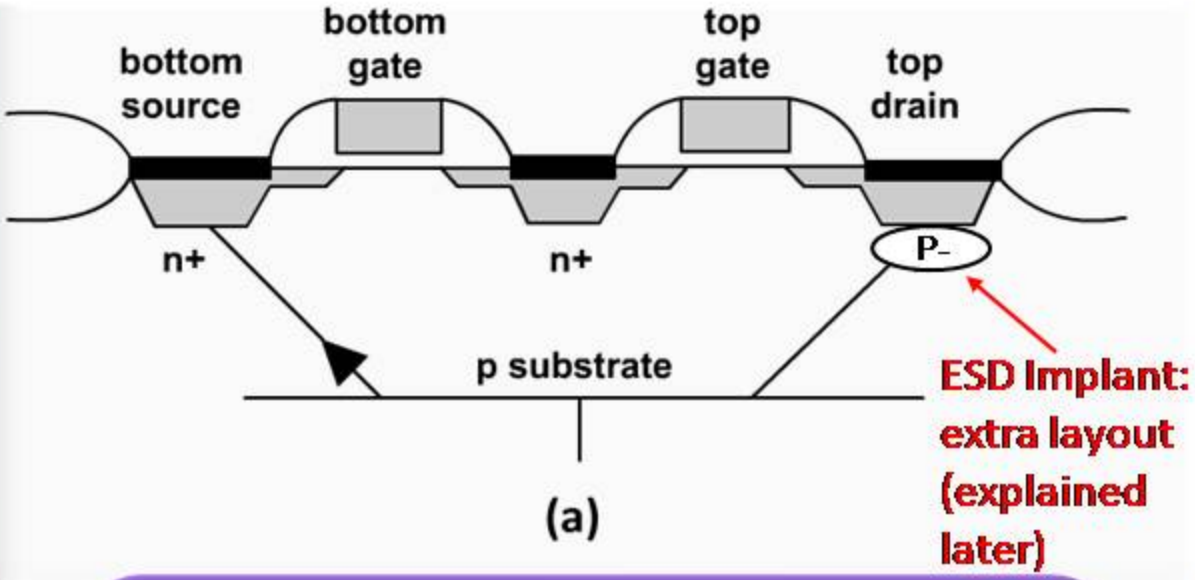
Typical I/O:

- Big size P1 as driving PMOS and ESD PMOS
- Big size N1 as driving NMOS and ESD NMOS

Cascade I/O:

- Floating substrate PMOS for well control
- Cascode NMOS for gate oxide reliability

Stacked (Cascode) NMOS



Wider base width than GGNMOS

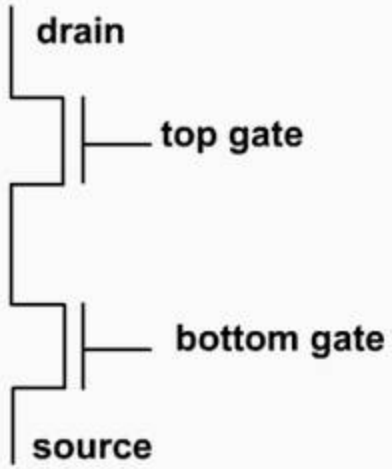


Figure 1 Stacked NMOS ESD structure in a silicided, LDD junction process:
(a) cross section,
(b) schematic diagram.

Stacked NMOS Voltage Operation

For 1.8V/ 3.3V 0.18μm application

Operation voltage 0- 5V (HVT: High-Voltage-Tolerance).

Vg = 3.3V

For pure ESD devices: the bottom gate grounded

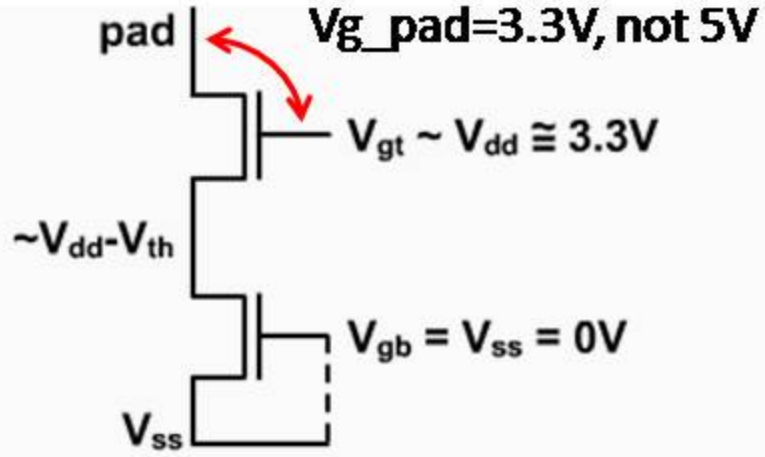


Figure2 Biasing the stacked NMOS ESD structure under normal circuit operation conditions.

Separated Driving and ESD Devices

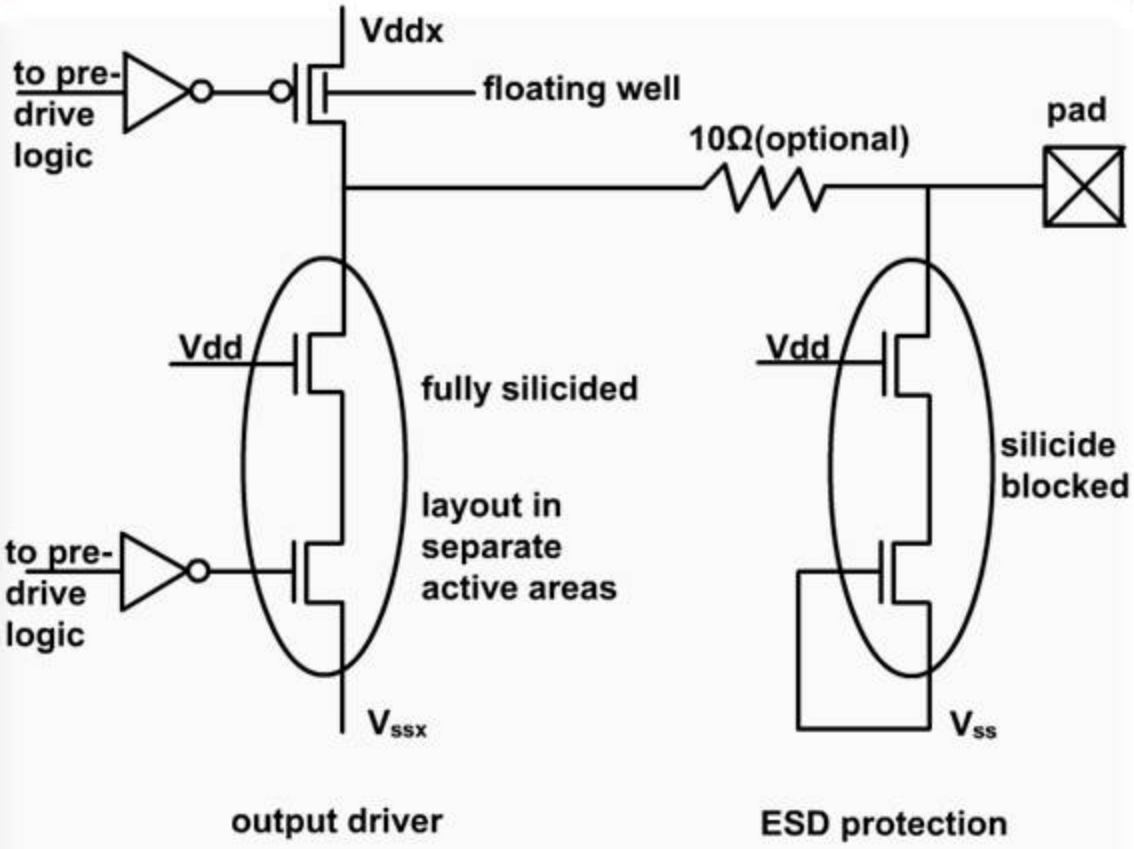


Figure 9 Schematic of stacked NMOS protection in a silicide blocked technology.

Disadvantage: Layout area consumption

Separated Output Driver Active Region

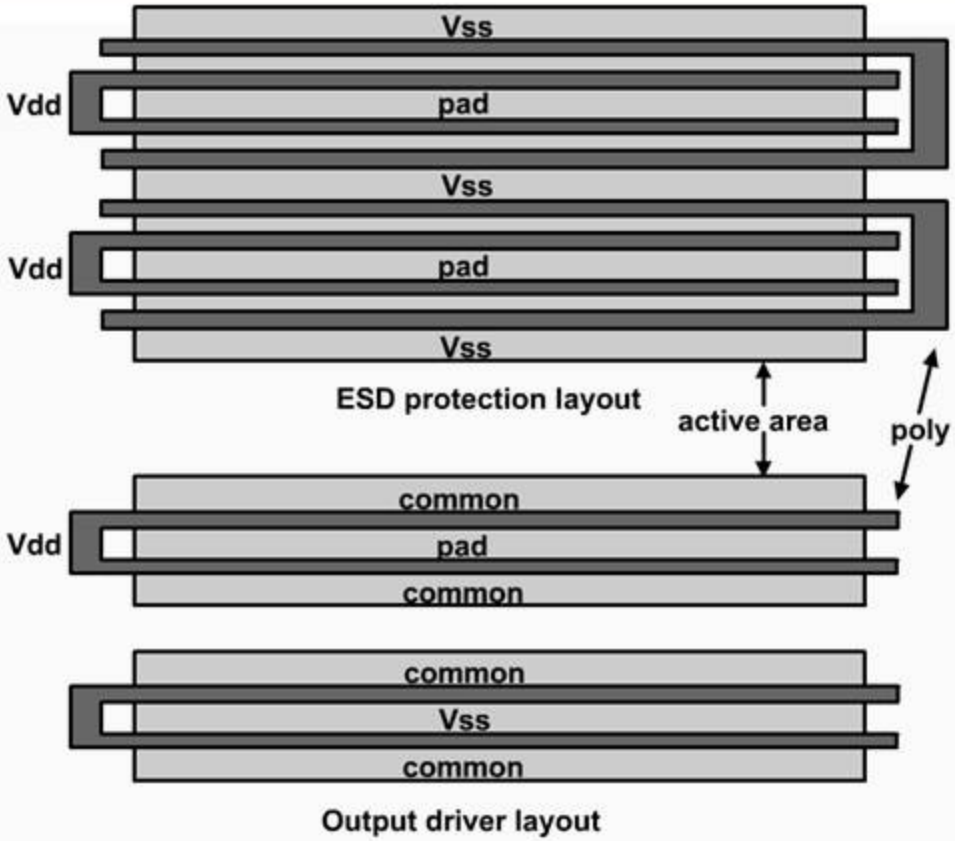
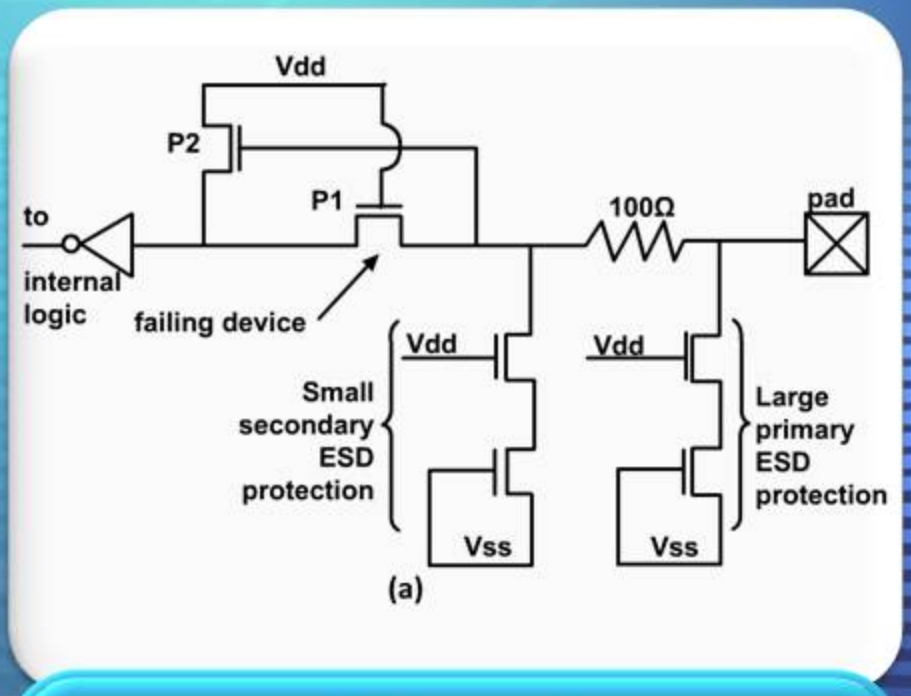


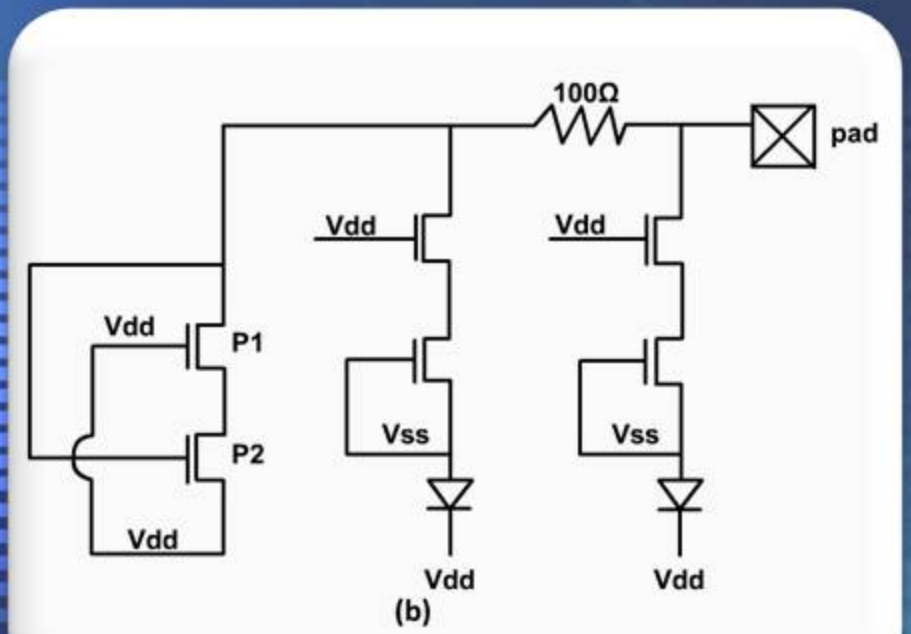
Figure 12 Stacked NMOS ESD protection (upper) layout in a single active area and stacked NMOS output deiver (lower) layout in seperate active areas. The metal connections between fingers are not shown.

Driving Device will not be easy to turn on.

Input Pass Gate



Schematic



Parallel discharge paths to Vdd

Input Pass Gate Correction

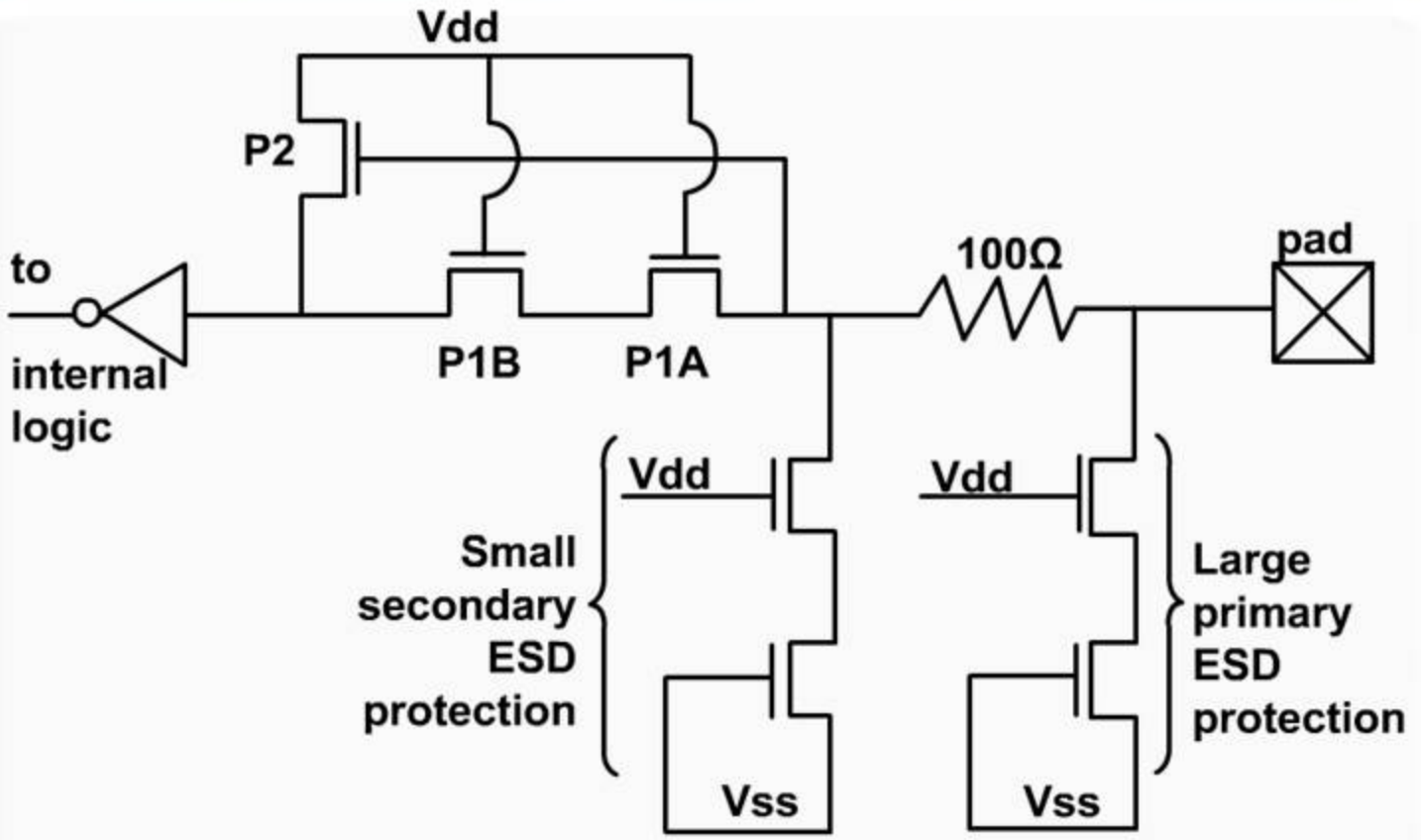


Figure 15 Correction to the input pass gate failure.

Change P1 to “P1A and P1B”.

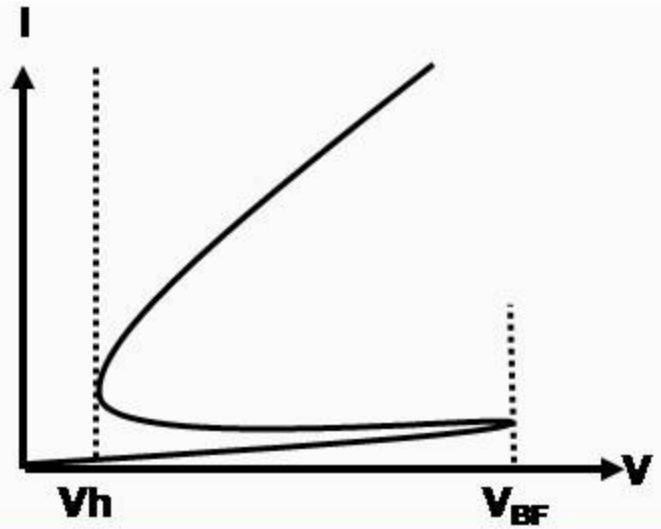
SCR Structure

Another pure-input ESD circuits

Target:

- VBF < Vbd_device (very hard)
- Vop < Vh (not induce Latch-Up)

Typical SCR structure



I-V Characteristics

SCR (Thyristor)

Advantages:

- Small Area
- Good ESD Performances

Disadvantages:

- Easy to induce Latch-Up
- Only can be input circuits
  (without output driving capabilities)

Thyristor

- Bistable Characteristics
- High-Impedance, Low-Current OFF State
- Low-Impedance, High-Current ON State

Thyristor

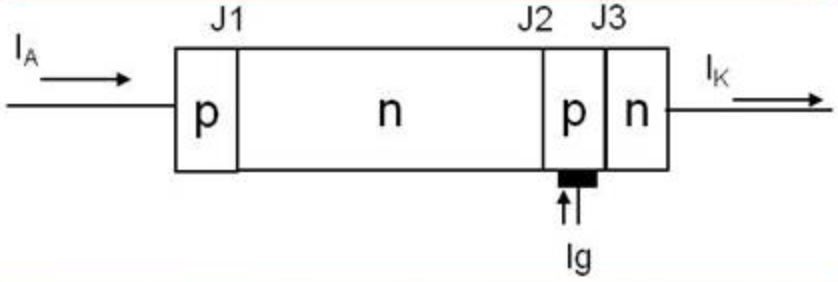
Two bipolars: p1-n1-p2 (α1); n1-p2-n2 (α2)

Three junctions: J1, J2, J3

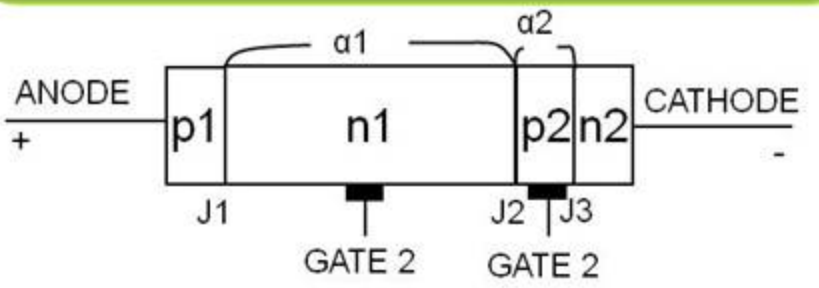
Two gates: gate1, gate2

Two-terminal p-n-p-n diode (Shockley diode)

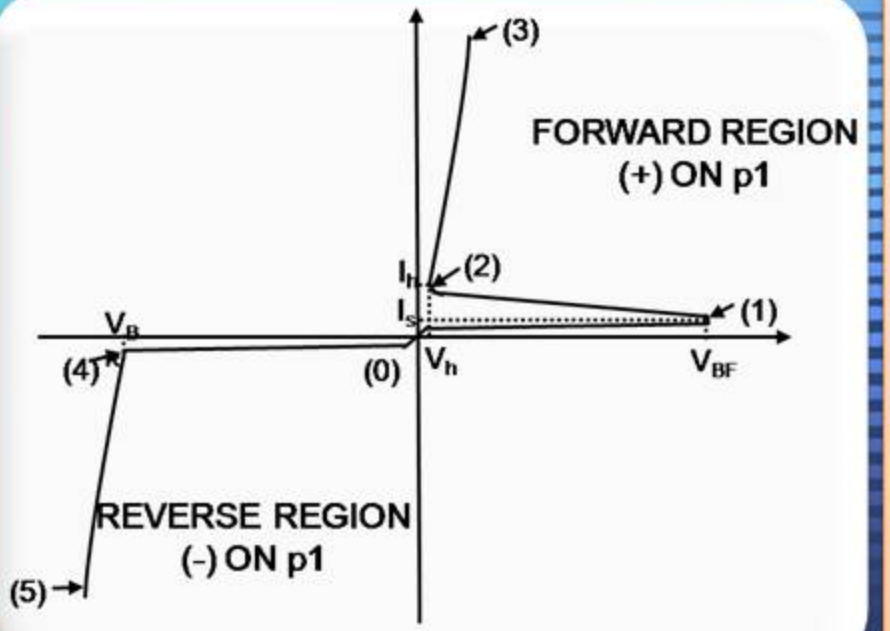
Three-terminal Thyristor



Four-terminal Thyristor



Current-voltage characteristics of a thyristor



- Region 0-1: forward blocking, OFF state, high impedance
- Point (1), a forward breakover voltage V_{BF}, a switching current Is (turn-on current), dV/dI=0
- Region 1-2: negative resistance
- Point (2), dV/dI=0 again, holding current I_h, holding voltage V_h
- Region 2-3: the forward conducting, ON state
- Region 0-4: reverse blocking state
- Point (4), a reverse breakover voltage V_{BR}
- Region 4-5: reverse breakdown region

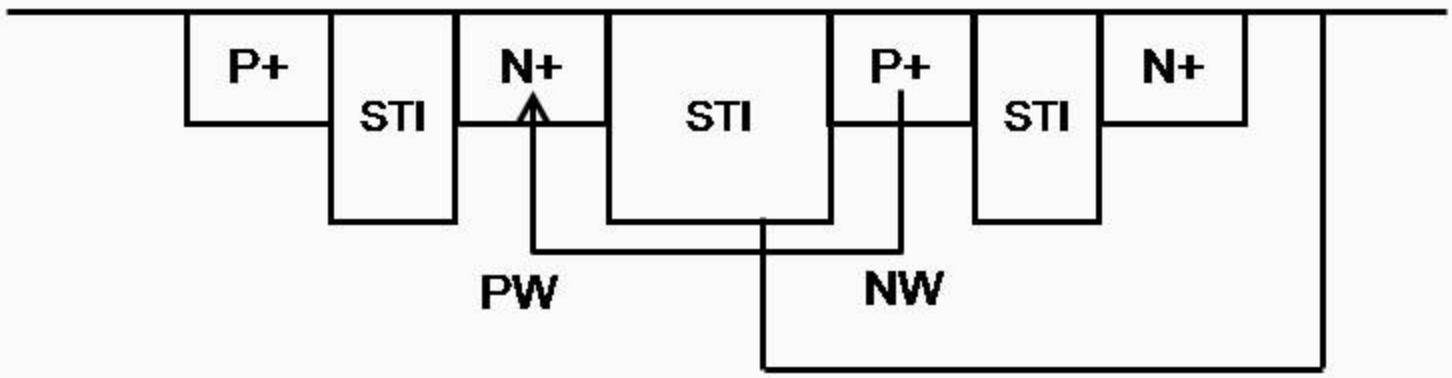
Lateral SCR (LSCR)

P+ of PMOS

PW of NMOS

NW of PMOS

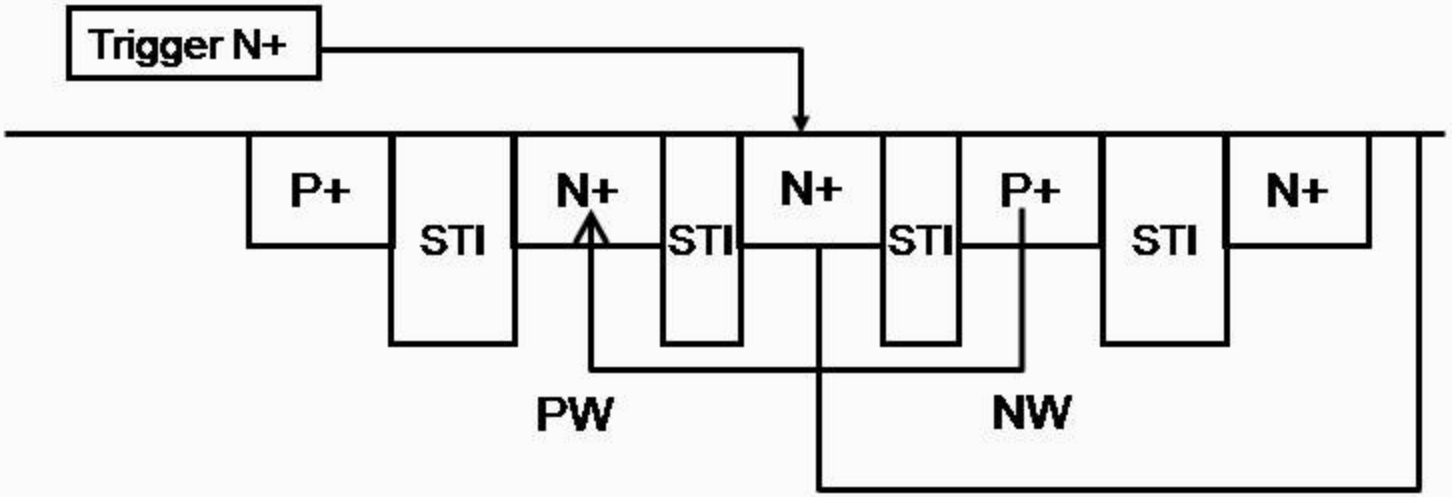
N+ of NMOS



Modified Lateral SCR (MLSCR)

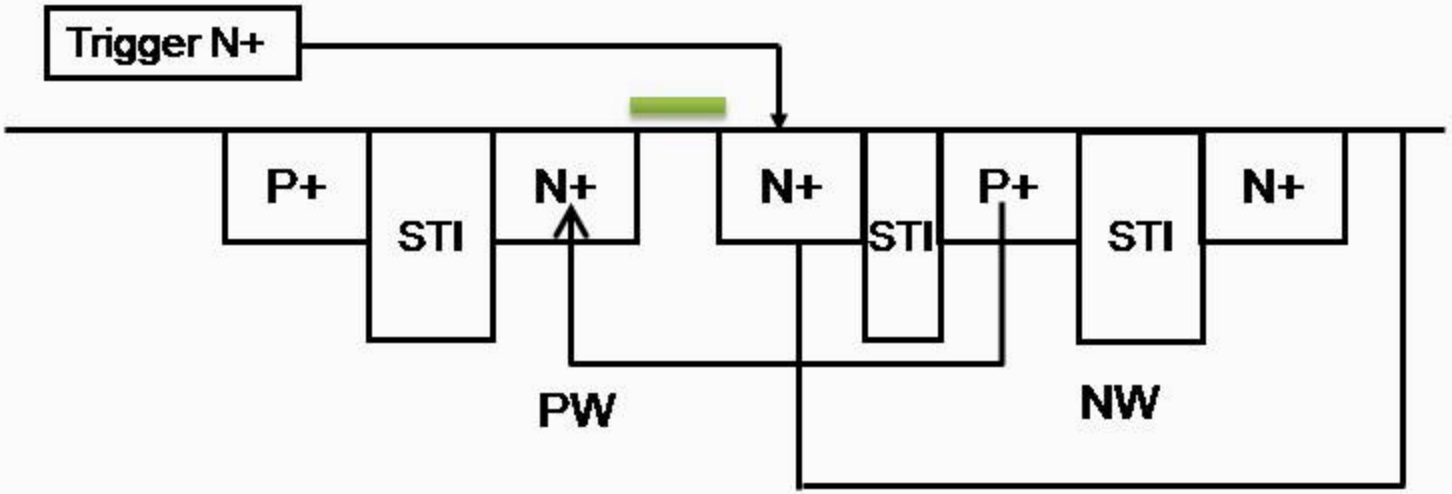
N+/PW junction breakdown provides a lower turn on voltage than the original PW/NW junction.

N+ could be replaced by P+ for P+/NW junction breakdown.



Low Voltage Trigger SCR (LVTSCR)

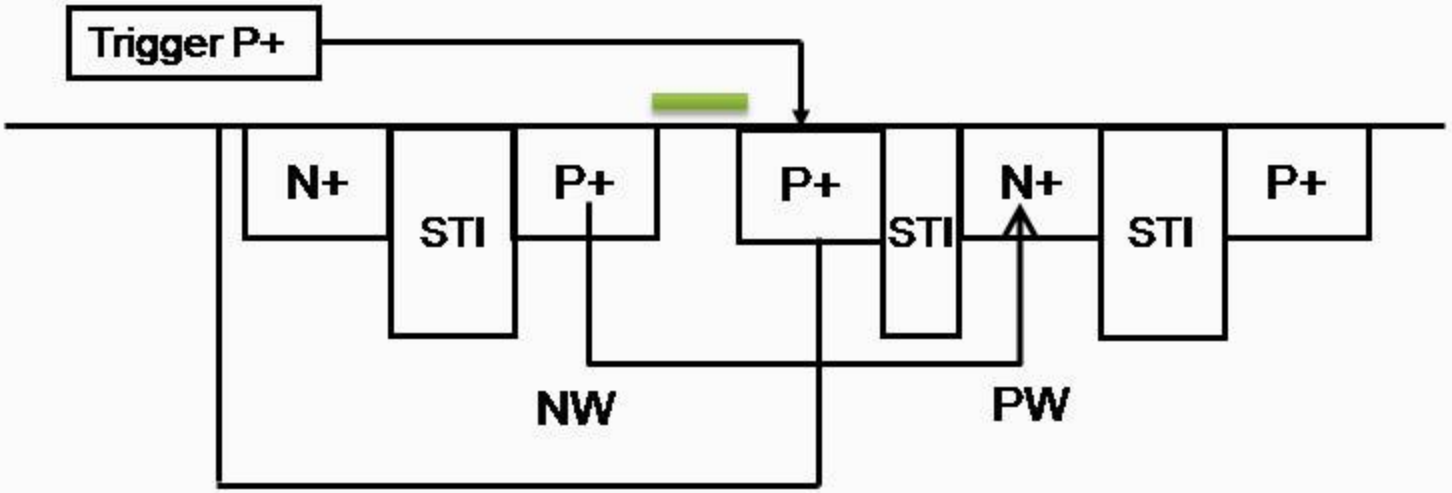
NMOS provides the currents to reduce SCR turn on voltage.



Low Voltage Trigger SCR (LVTSCR)

PMOS provides the currents to reduce SCR turn on voltage.

Hole mobility is only half of electron, so NMOS triggering should be better.



Two Kinds of Typical Trigger Circuits

Advantages:

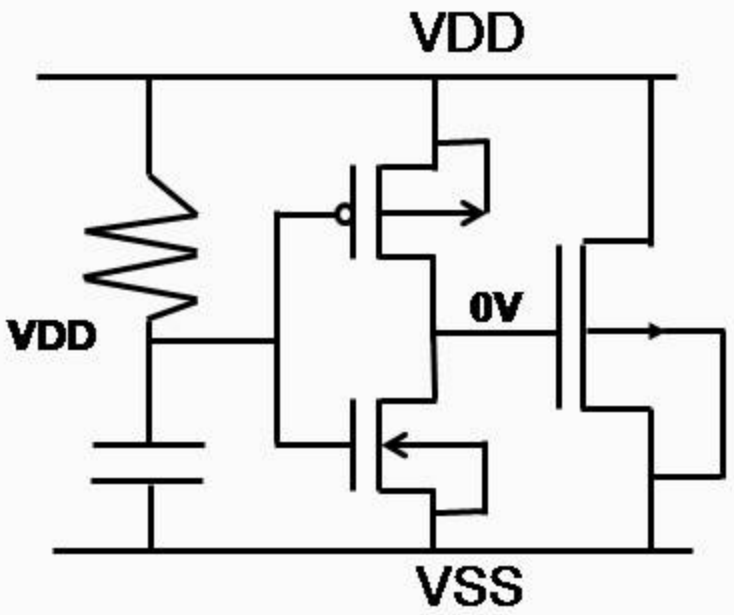
- Make ESD protections turn on fast.

Disadvantages:

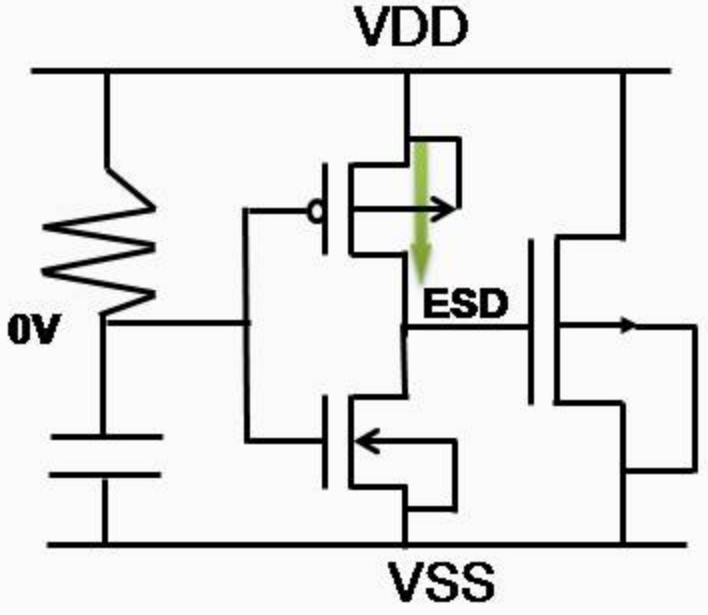
- Add layout areas.
- Add power-on leakage currents.

Surface-Trigger (Gate-Driven) Circuits

Normal operation after RC time constant



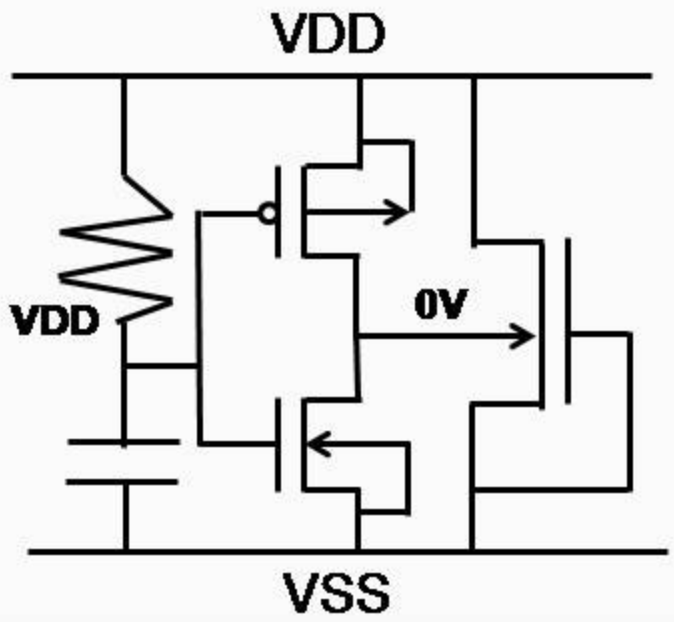
ESD zapping before RC time constant



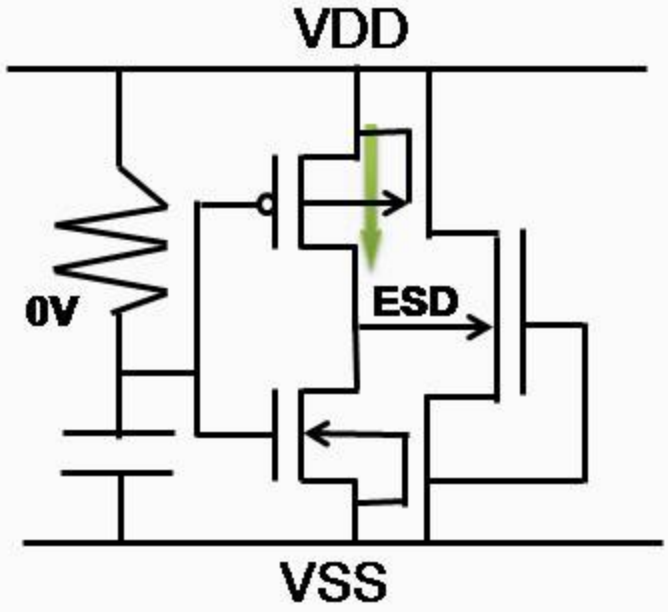
ESD: low ESD turn-on voltage

Substrate Trigger Circuits

Normal operation after RC time constant

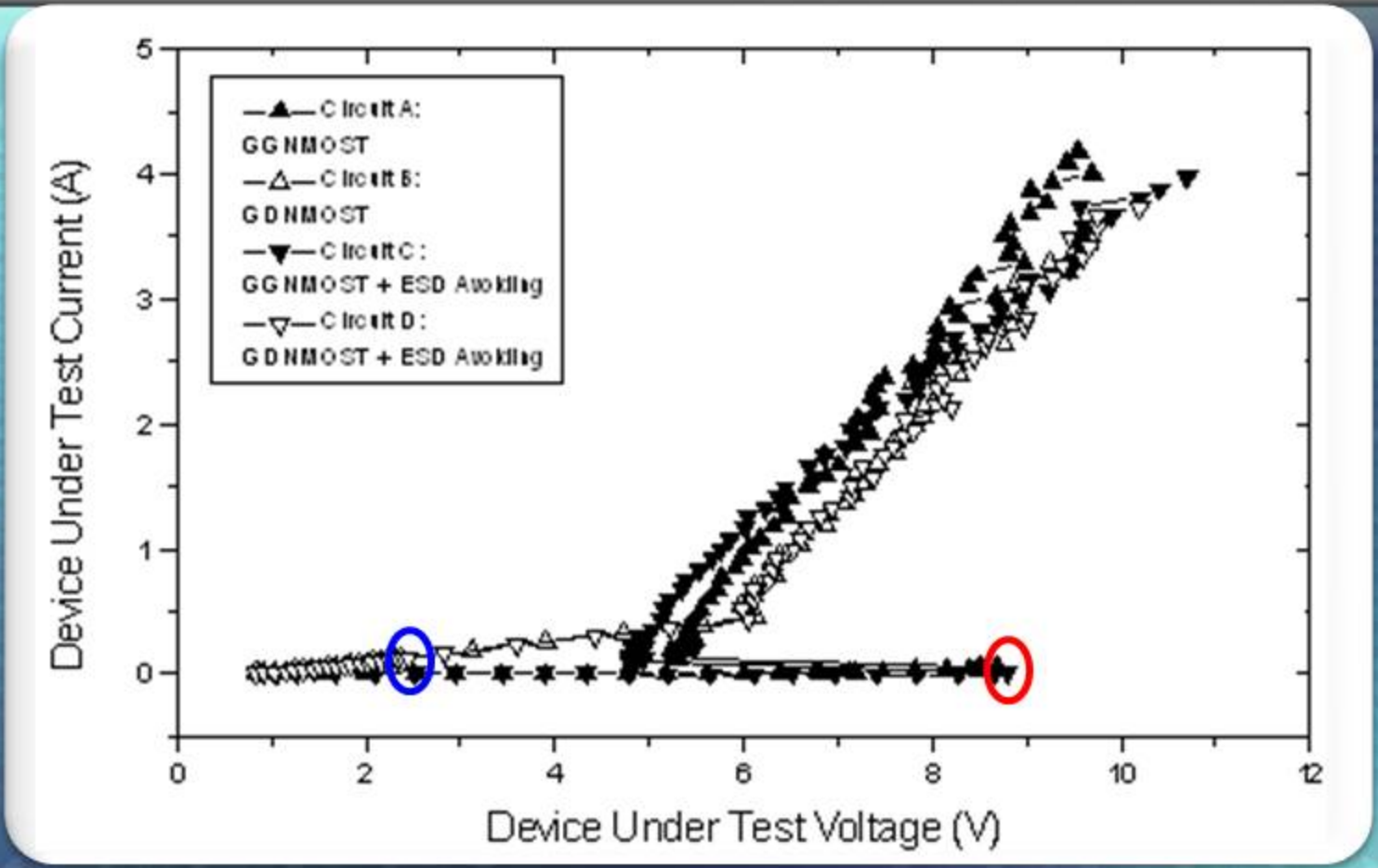


ESD zapping before RC time constant



ESD: low ESD turn-on voltage

Silicon Data



Circuits A and C (GGN): large triggering-on voltage

Circuits B and D (Gate-Driven): small triggering-on voltage

Schmitt Trigger Circuit Weak Points

ESD test: zap at VDD with grounding VSS

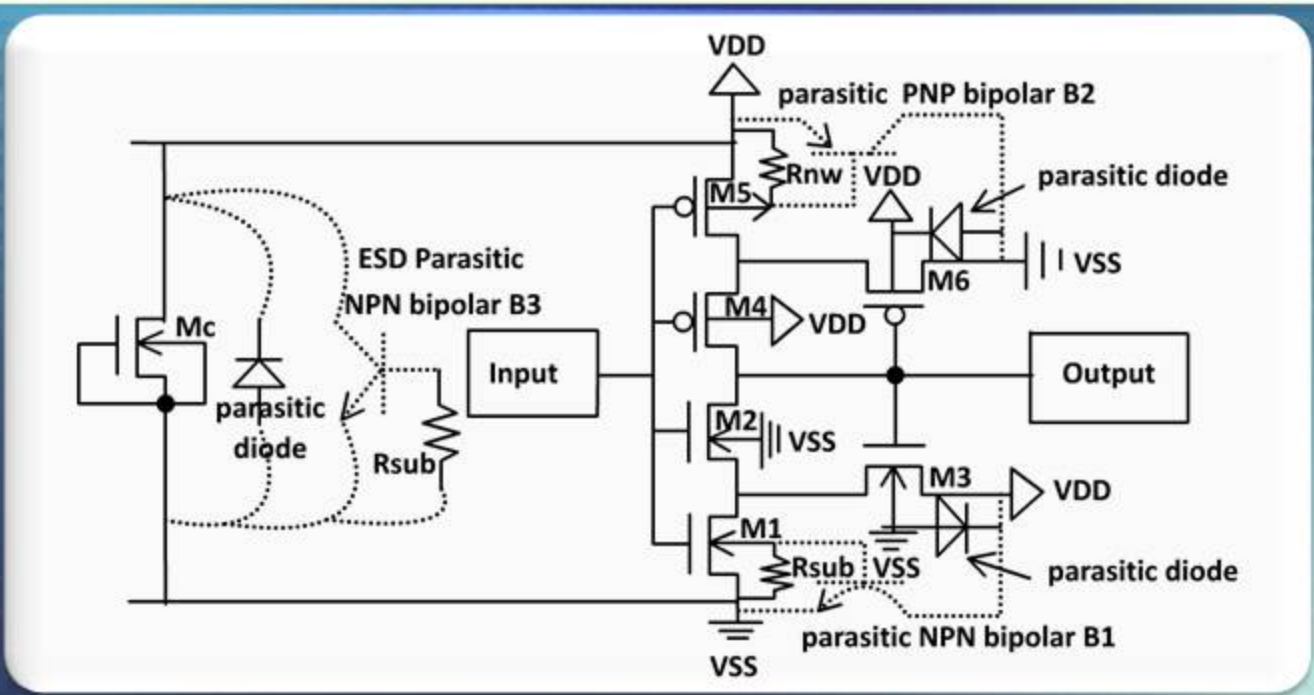
ESD protection: Mc

PMOS parasitic bipolar: B2 (PNP), small size

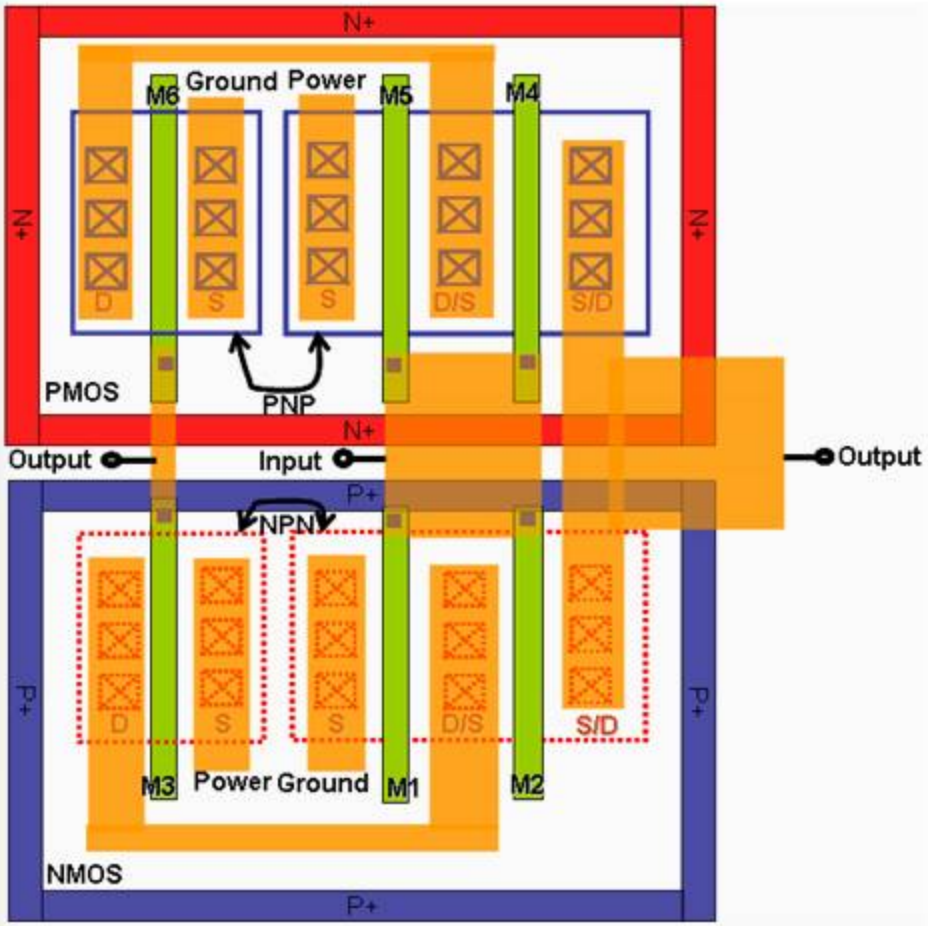
NMOS parasitic bipolar: B1 (NPN), small size

Good ESD: Mc turning on without B1/B2 turning on

The base of PNP/NPN larger than the base of the parasitic NPN bipolar in Mc

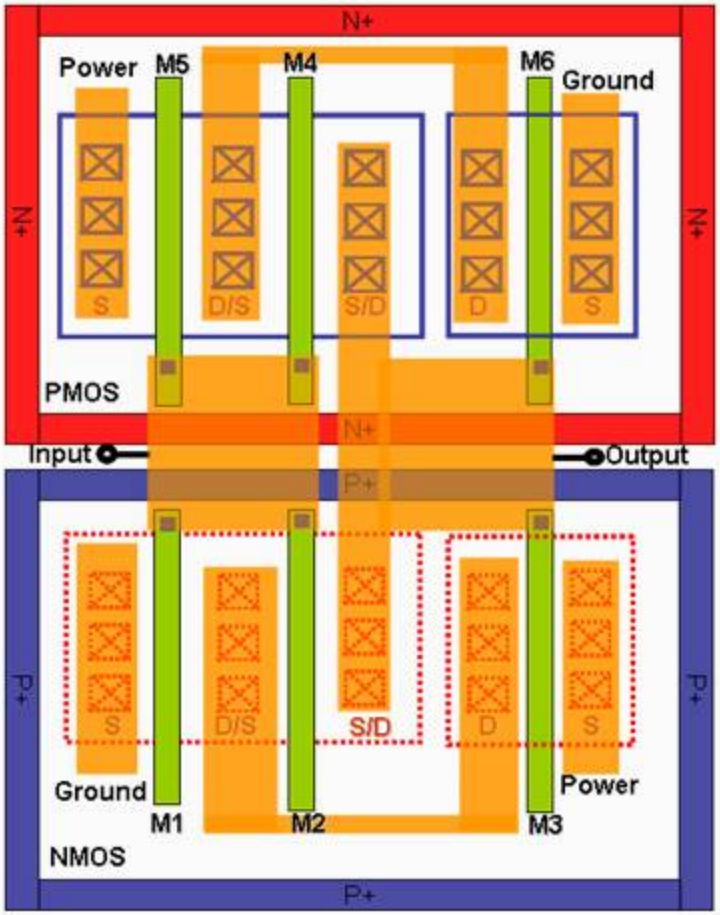


Wrong Schmitt Trigger Circuit Layout



- PNP between Power and Ground
- NPN between Power and Ground
- Small size
- Large leakage currents from Power to Ground after ESD stresses

Correct Schmitt Trigger Circuit Layout



A large base PNP between Power and Ground

A large base NPN between Power and Ground

ESD NPN turning on before the small PNP/NPN turning on

Full Chip ESD Protection

There are ESD paths between Two Terminals

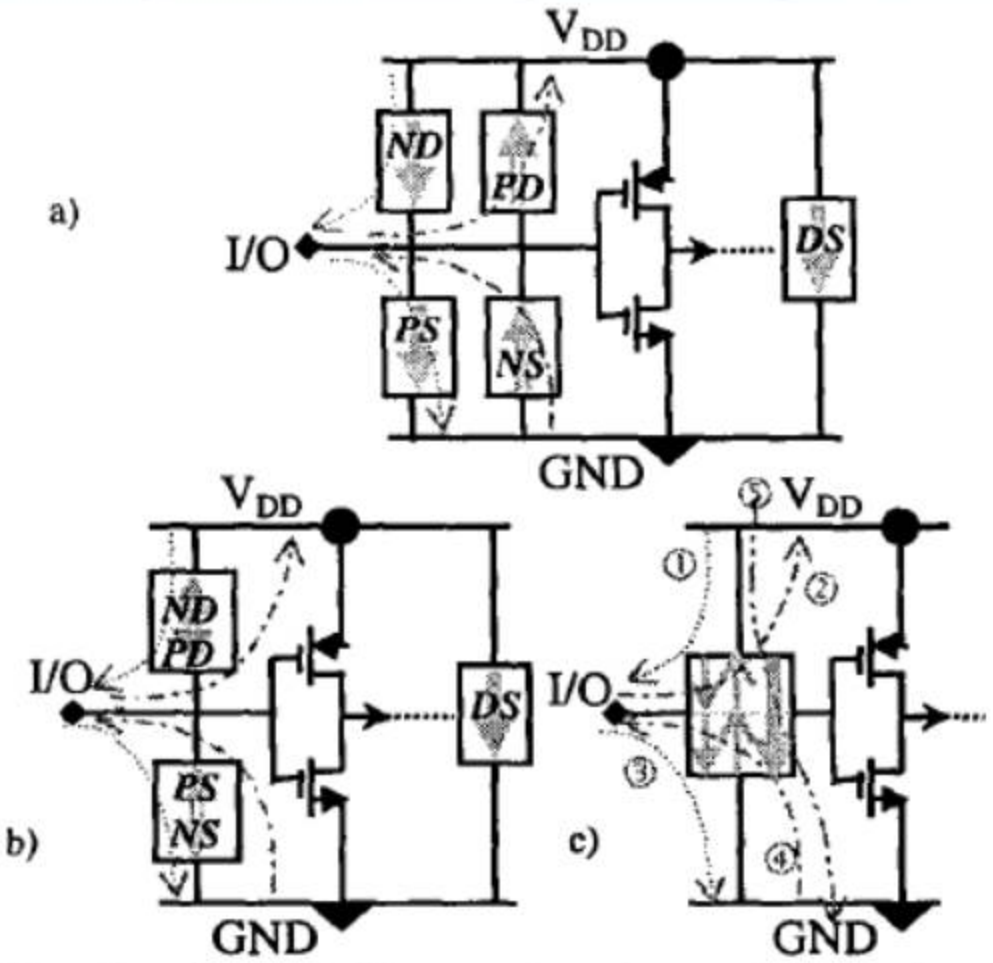


Fig. 1 Complete all-active ESD protection schemes:a) Five devices; b) three devices; c) This work-one device. ①=ND, ②=PD, ③=PS, ④=NS, ⑤=DS.

Full Chip ESD Protection

A/D interface:

- ESD test: Vdda- Vssd
- ESD currents can damage the cross devices.
- Solutions:
  - Avoiding such internal cross devices
  - Adding ESD devices

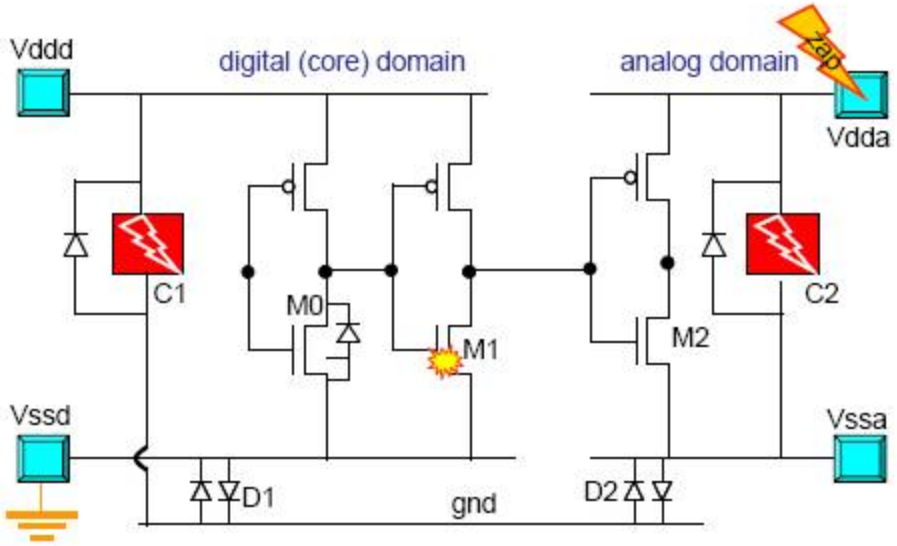
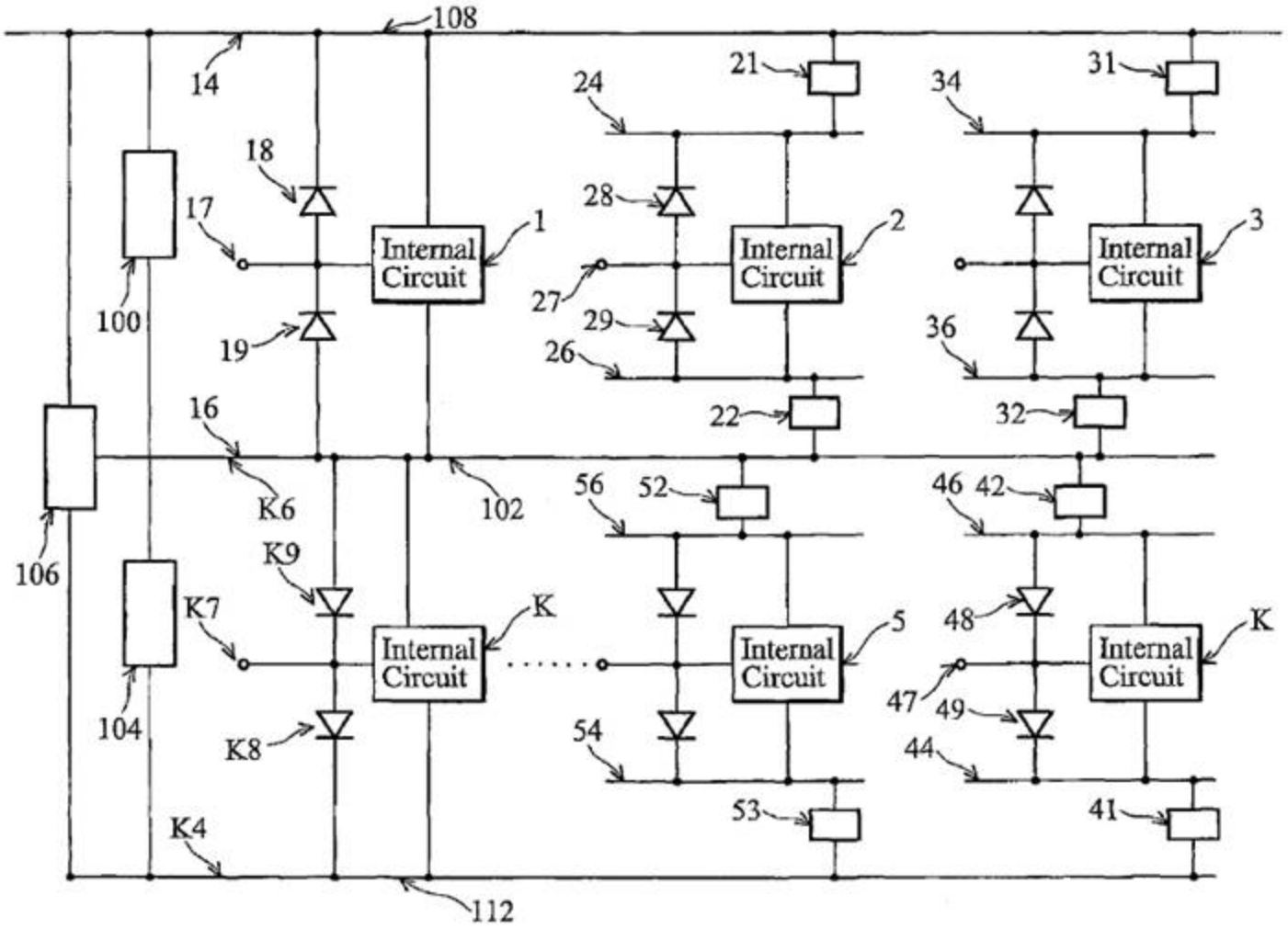


Figure 1 Failure during cross-domain stressing from Vdda to Vssd.

One VDD Bus as ESD Bus

VDD Bus= VDD1 or VDD2 or VDD3



Metal Routing

Make ESD currents flowing uniformly

Path A = Path B

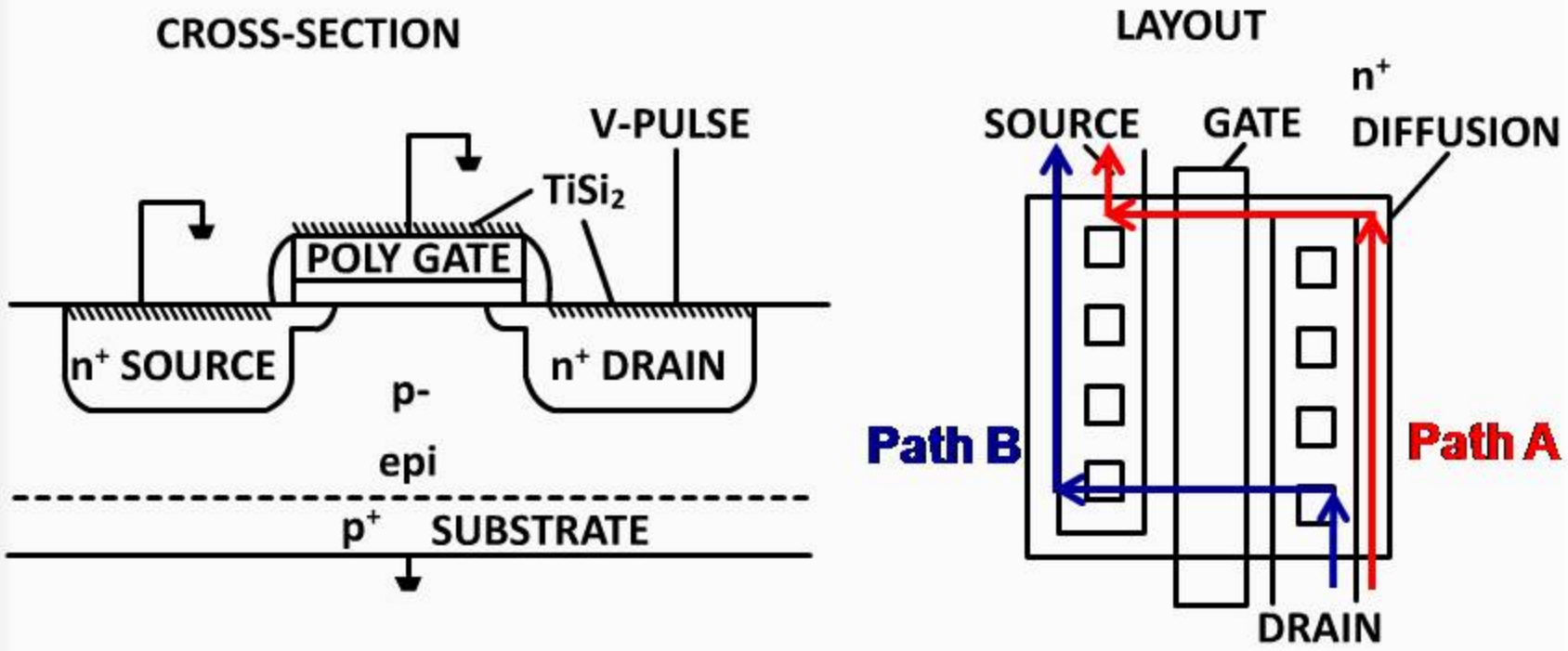


Fig. 1. Cross section and layout of the single-poly n-MOS device.

Process Impacts on ESD

Two methods can be applied to add ESD robustness.

The first one is to keep away the weak path (or devices) from ESD zapping (process impact).

- Salicide Blocking
- ESD Implant
  - Without LDD (Lightly Doped Drain)
  - P+(P-) under N+

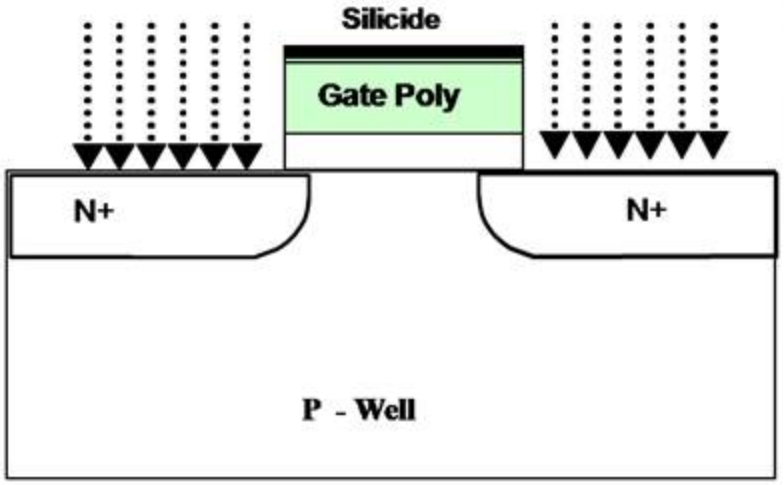
The second one is to increase ESD bypass channels.

- ESD circuit

ESD Implant

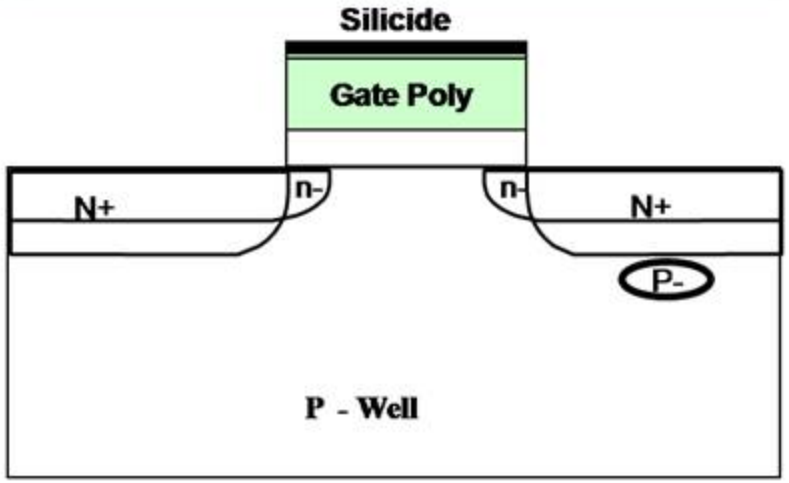
ESD Implant before spacer (without nLDD)

- Reducing the weak points
- Not used in the advanced technologies



PESD implant

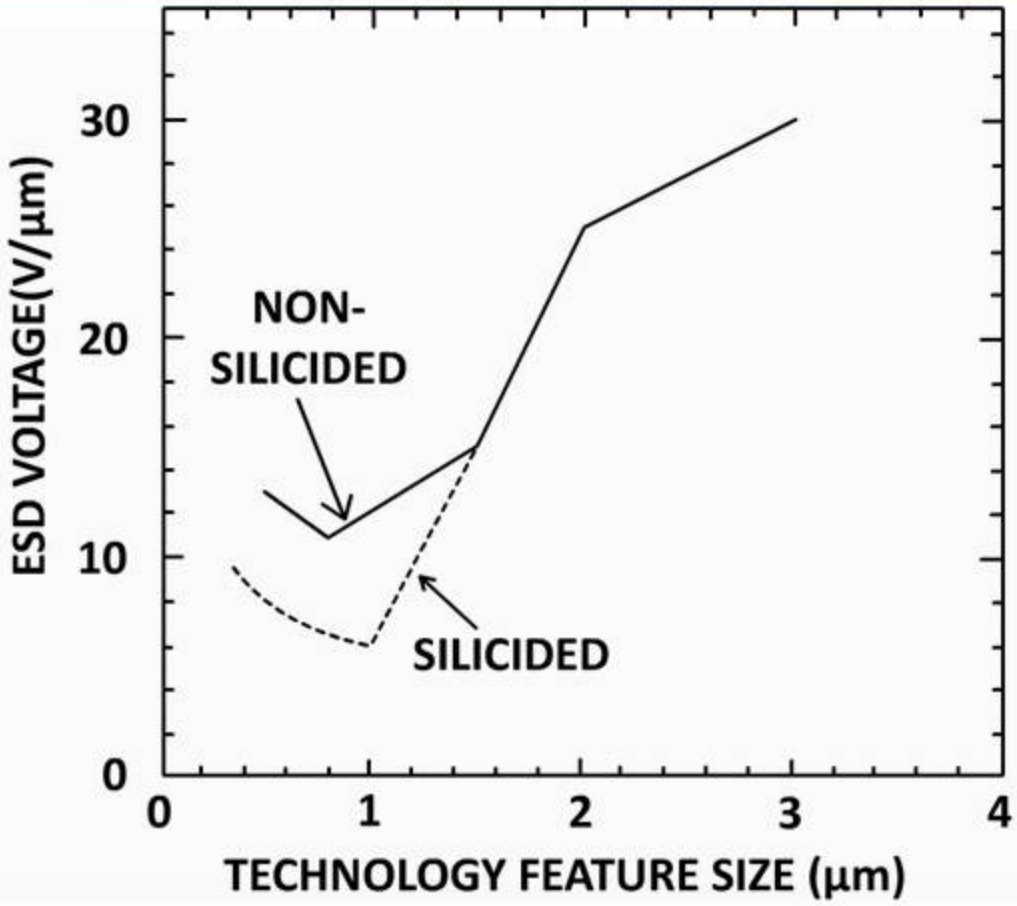
- Dosage: (PW)< (P-) < (P+)
- Changing the junction breakdown from N+/PW to N+/P-
- Advantage: reducing the drain junction breakdown voltage => very powerful ESD improvement
- Disadvantage: One extra mask



Silicide Effect

In old technologies: V_esd with silicided = V_esd with non-silicided

In new technologies: V_esd with silicided << V_esd with non-silicided



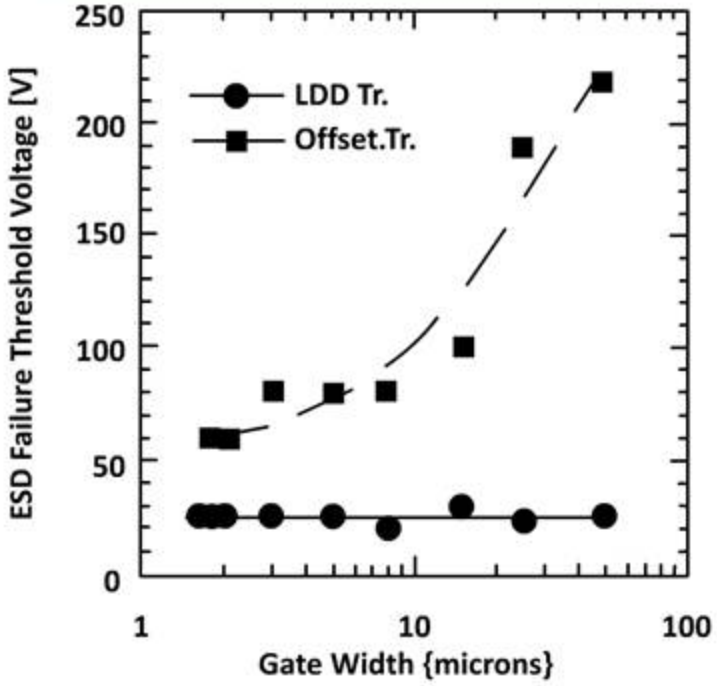
ESD performance of a gate-coupled nMOS device in V/µm as a function of the technology feature size. The effect of silicided and non-silicided technologies is clearly shown.

LDD Effect

Gate Width dependency of ESD Property :

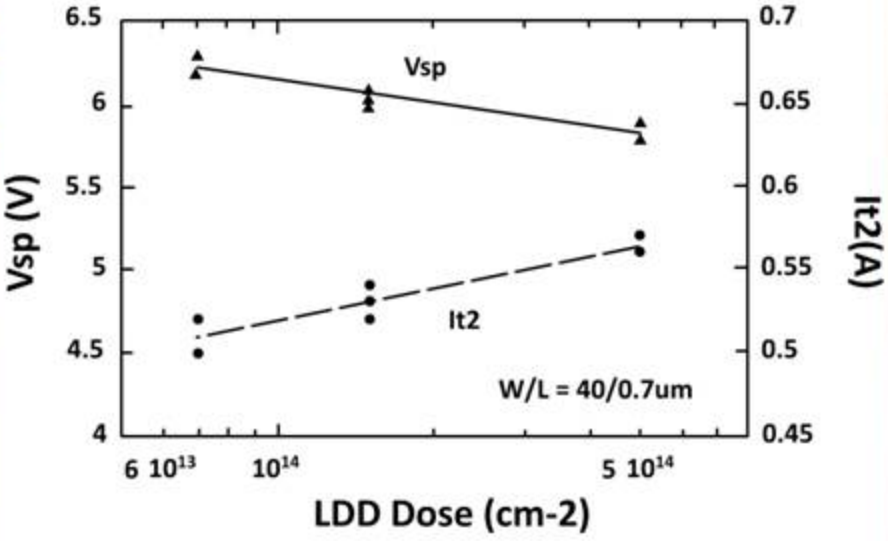
LDD Tr. : very bad ESD

Offset Tr.: ESD increasing as gate width added



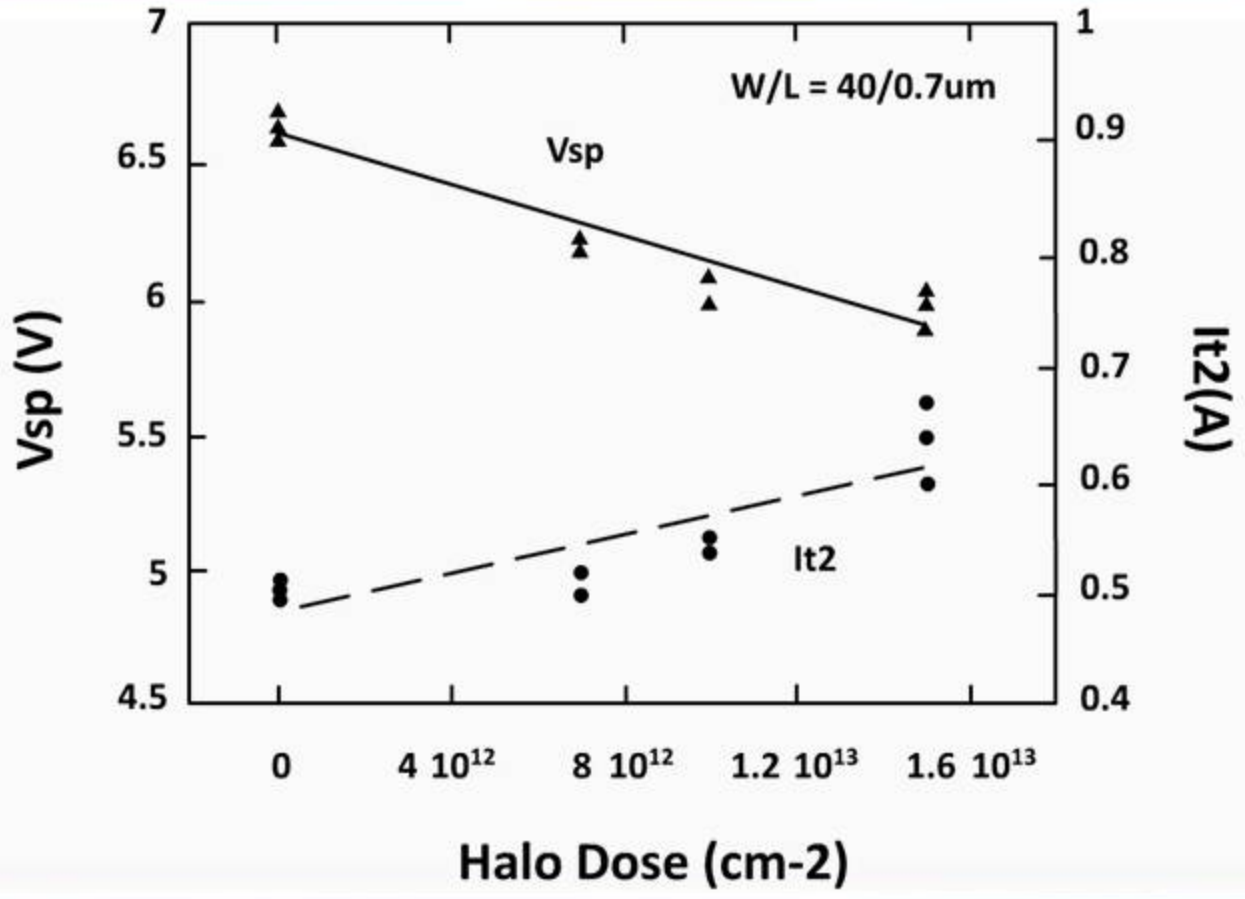
It2 and Vsp versus arsenic nLDD dose:

LDD Dose ↑ => Vsp ↓ => It2 ↑



Halo Effect

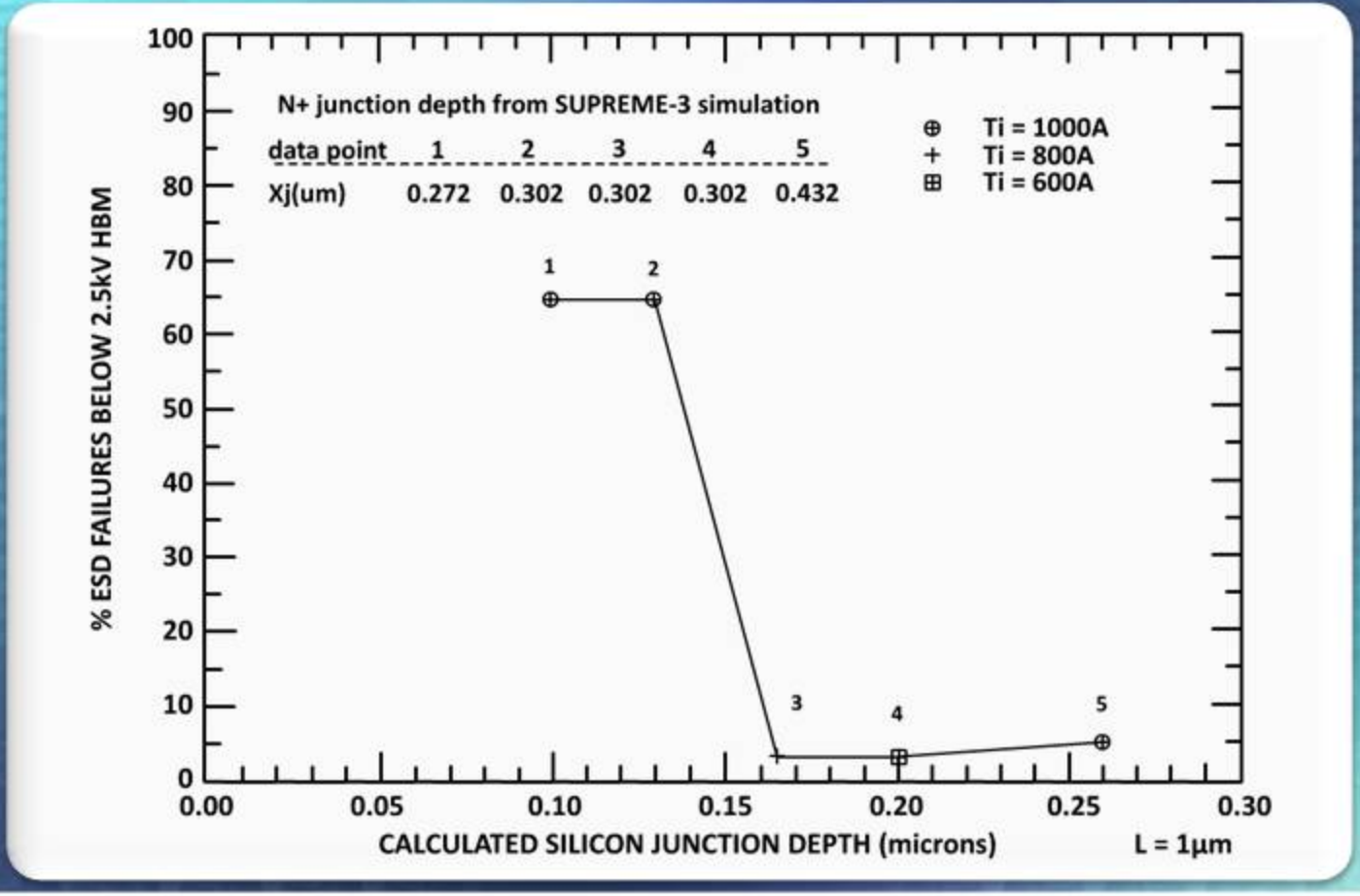
High dose => Low Vsp => High It2



It2 and Vsp versus boron halo implant dose

Junction Depth Effect

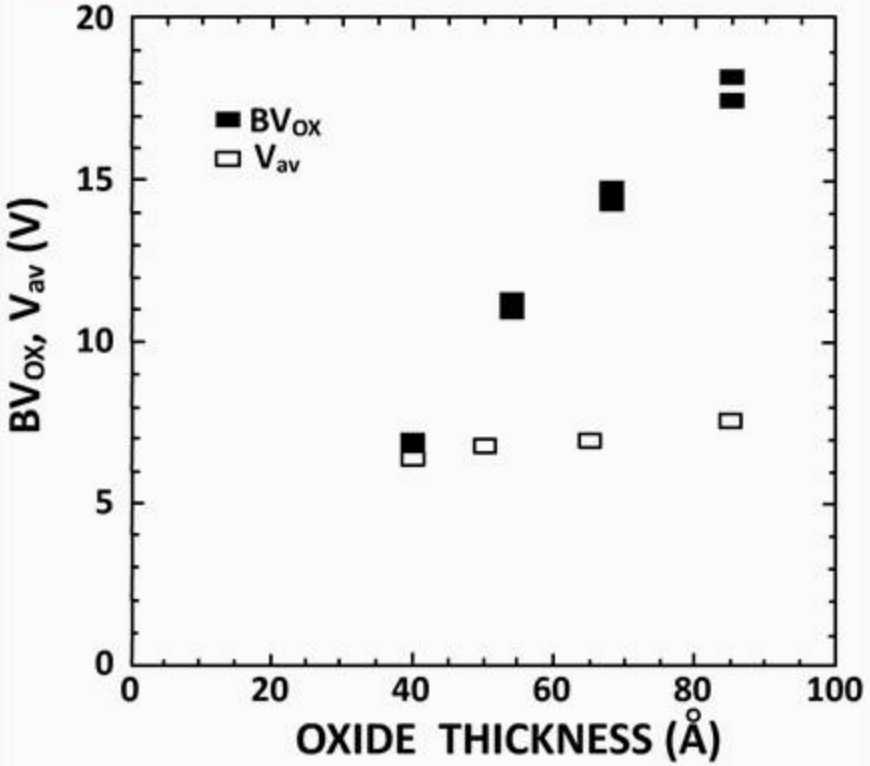
Large Depth => Low ESD failure below 2.5kV



The percentage of devices which fail below 2.5kV HBM as a function of calculated silicon junction depth Xjs

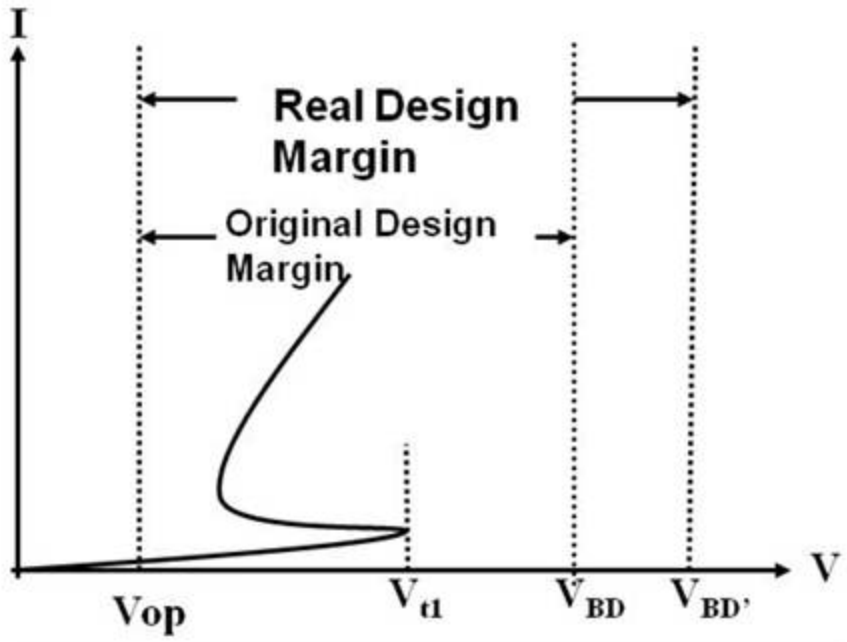
Gate Oxide Effect

Smaller the oxide thickness is, smaller the breakdown voltage will become.



Oxide breakdown voltage, BVox as a function of oxide thickness

ESD oxide breakdown voltage is larger than the DC BVox .



ESD Test

Test Procedures

- Define IC pins : Power, Ground, Input, Output and I/O.
- Define zapping and grounding pins.
- Choose zapping events: HBM, MM or CDM.
- Design which pins to trace I-V curves.
- Classify failure criteria.

ESD Failure Criteria

Short and open test

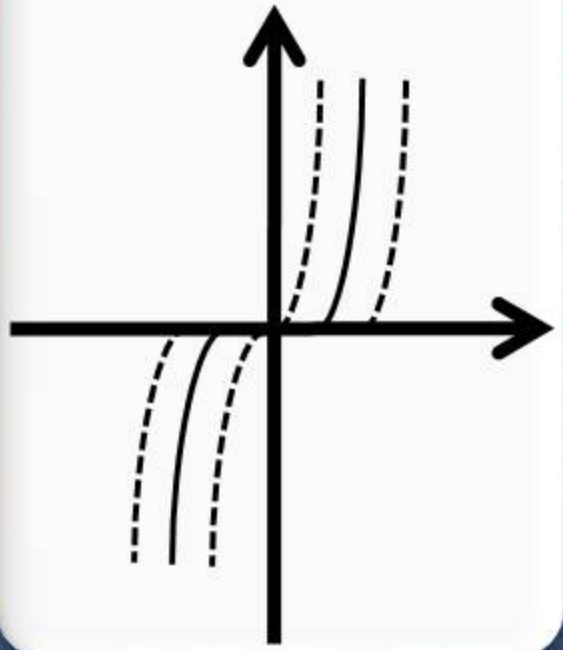
Diode test (fail if current smaller (larger) than the setting value at specified voltage)

I-V curve verification

- I-V envelope: the envelope of I-V curves is the criterion. Devices fail if the I-V curves drift outside the setting range behind ESD stress.
- Absolute leakage: device current must be below one designated number at specified voltage.
- I-V comparison: define that currents can't be over specified percentage at one assigned voltage.

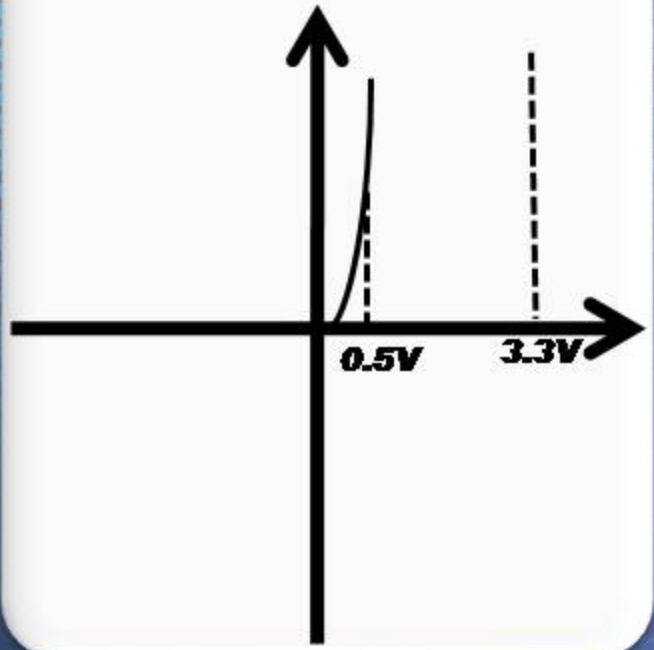
I-V Curve Verification

I-V envelope



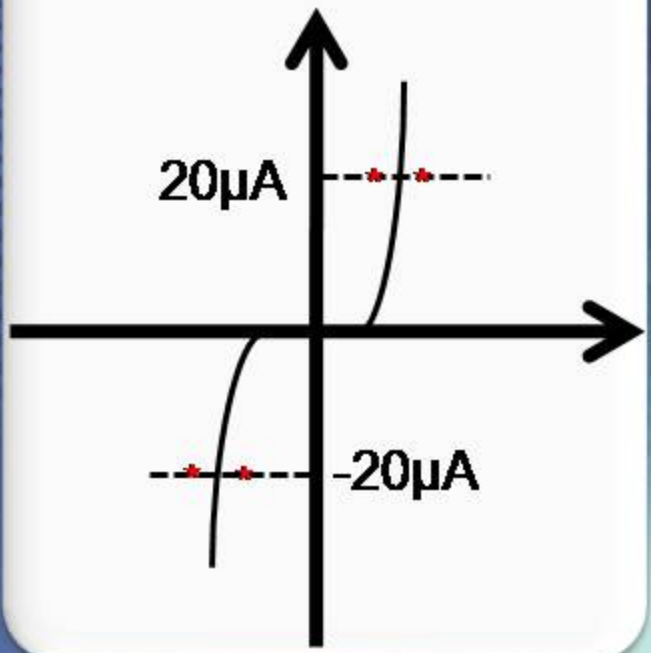
Absolute leakage:

- Ex: I< 0.1µA @ V=3.3V



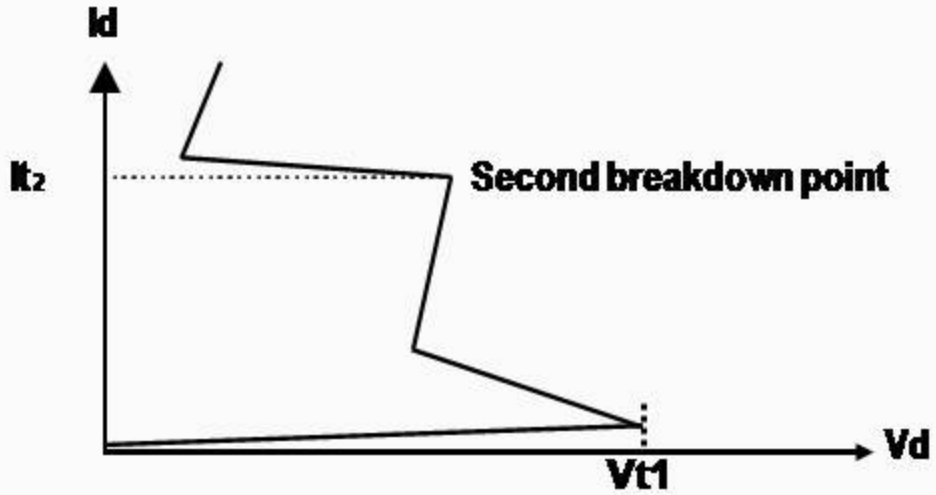
I-V comparisons:

- Ex: V shift < 10% @ I= +/- 20µA



TLP(G): Transmission Line Pulse (Generator)

Introduction to the TLPG measurement

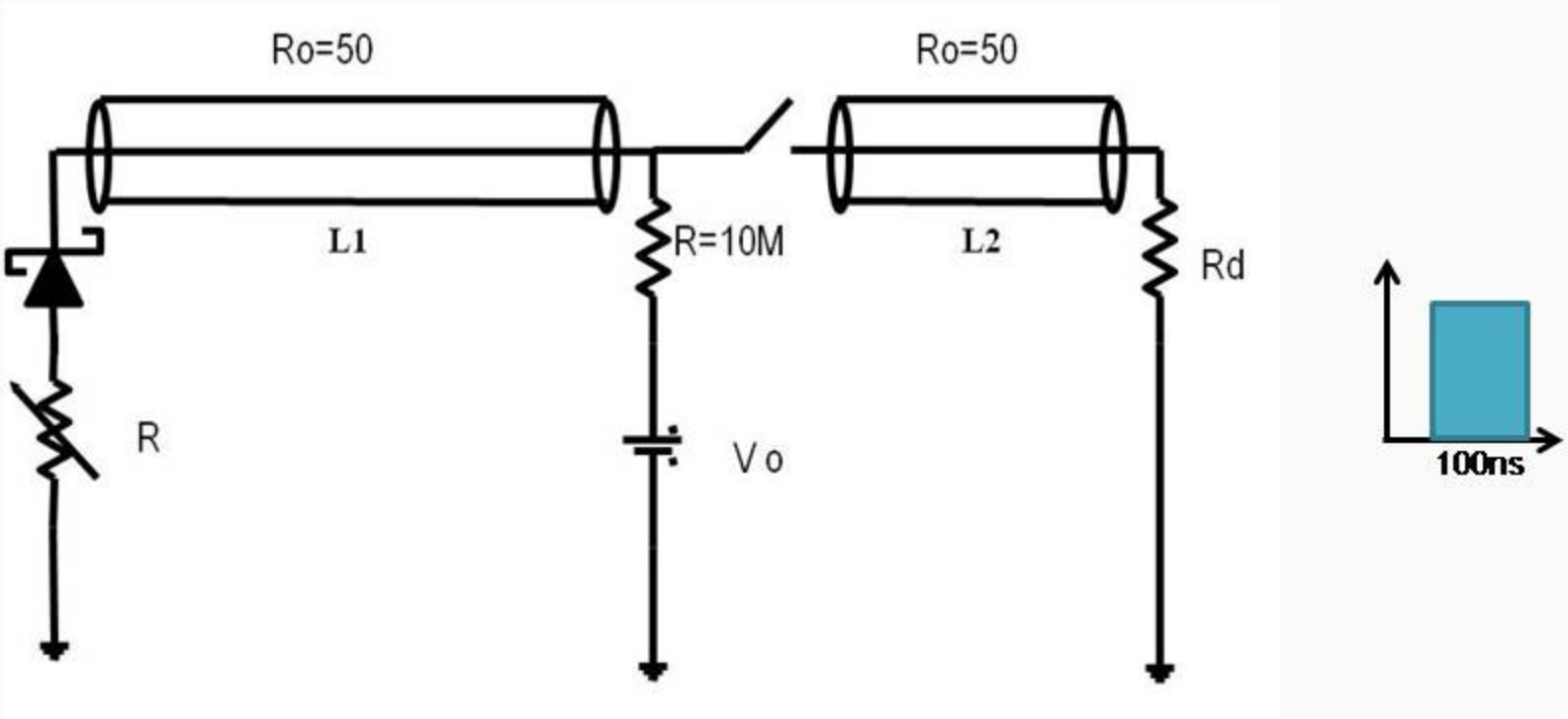


- V_{ESD} : ESD robustness voltage
  I_{t2} : second breakdown current
- The ESD model : $V_{ESD} = I_{t2} * (R + R_{device})$
- TLPG test : measuring the I_{t2} by using the TLPG system

Introduction to the TLPG measurement

TLPG equivalent circuit:

- Two 50Ω cables
- One 10MΩ resistor
- Simple model: 100ns square waveform



Test Machine Scheme

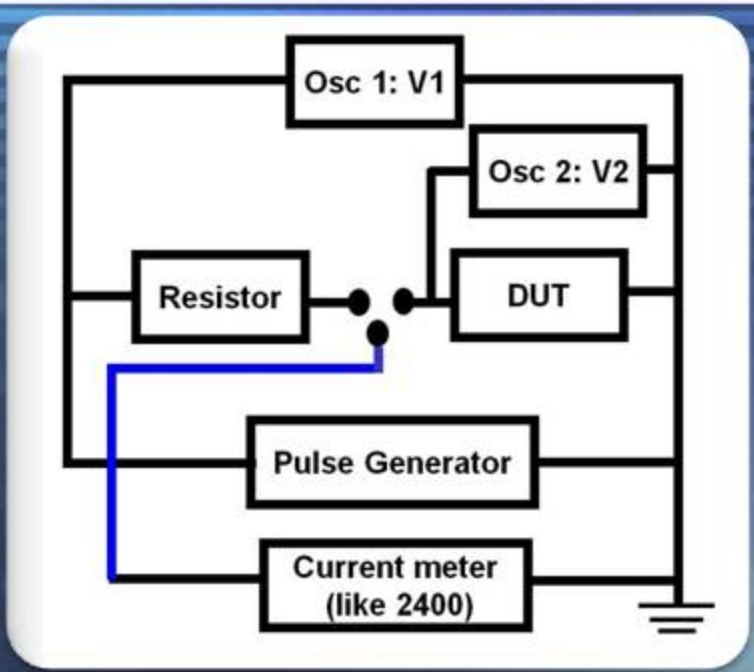
Osc. 1 (V1): measuring the device current (=V/R)

Osc. 2 (V2): measuring the device voltage

Pulse generator: providing the pulse voltage

Current meter: measuring the stand-by current (off current)

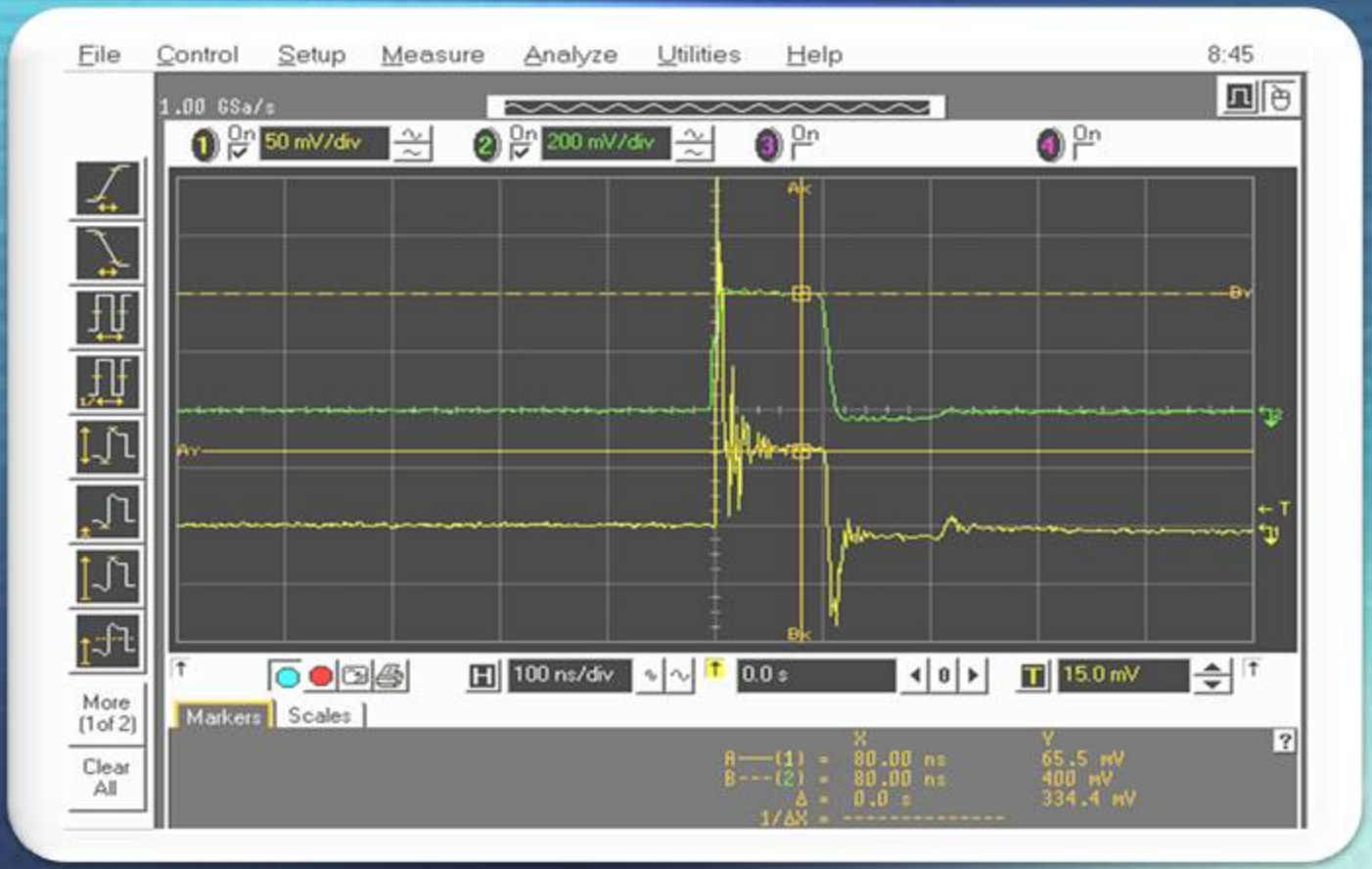
Pulse Generator => current meter => pulse generator => current meter ... (till the stand-by current larger than the failure criterion)



Testing procedures of experiments

Current waveform of the DUT before second-breakdown
(Osc. 1: yellow waveform, I=V/R)

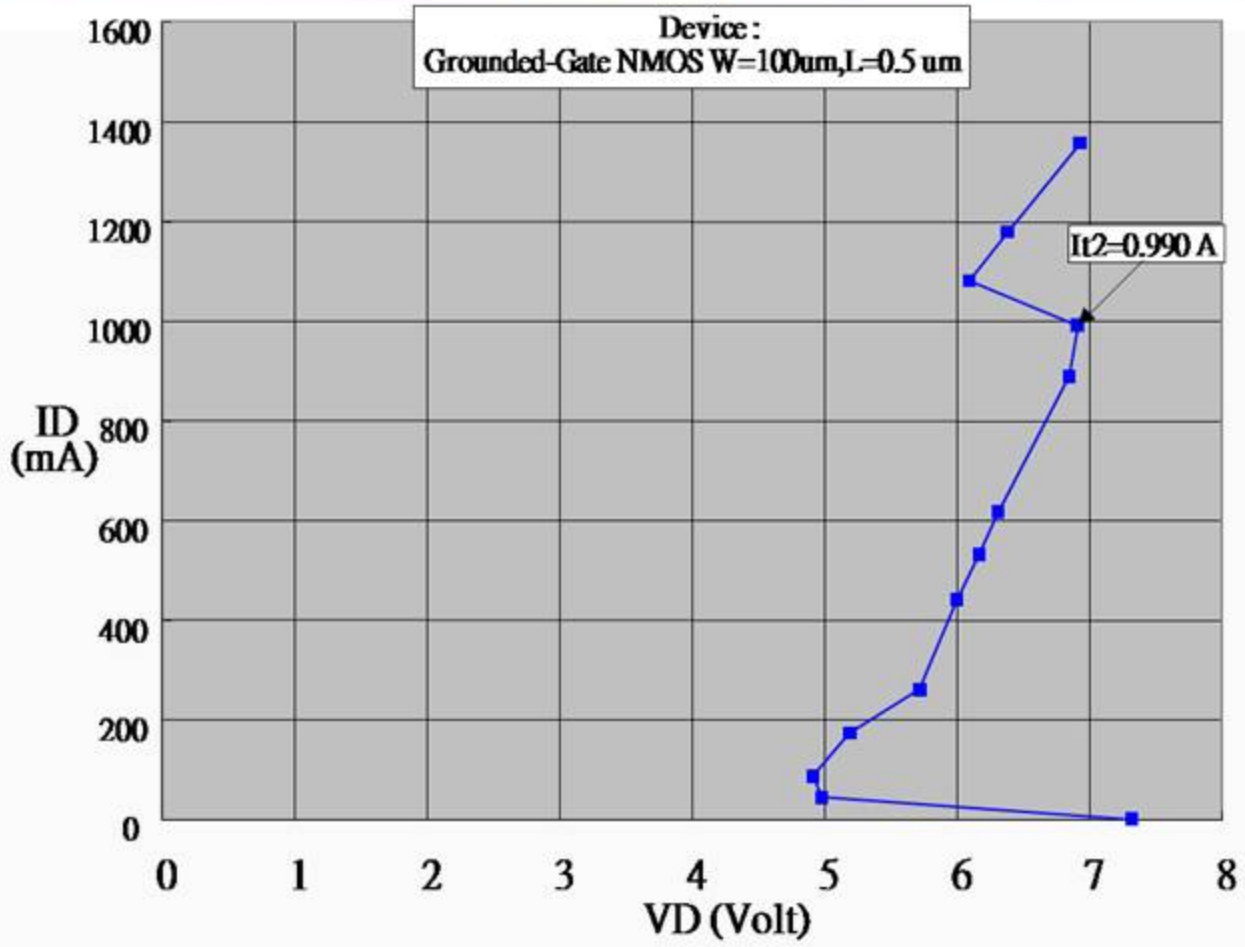
Voltage waveform of the DUT before second-breakdown
(Osc, 2: green waveform)



Experimental results

GGNMOS

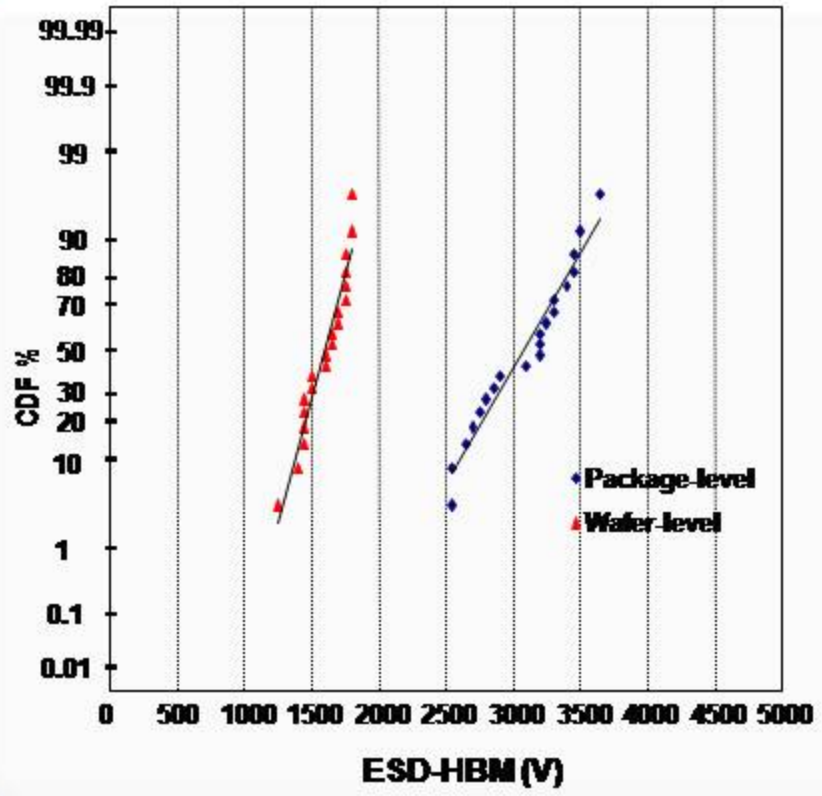
One-point by one-point

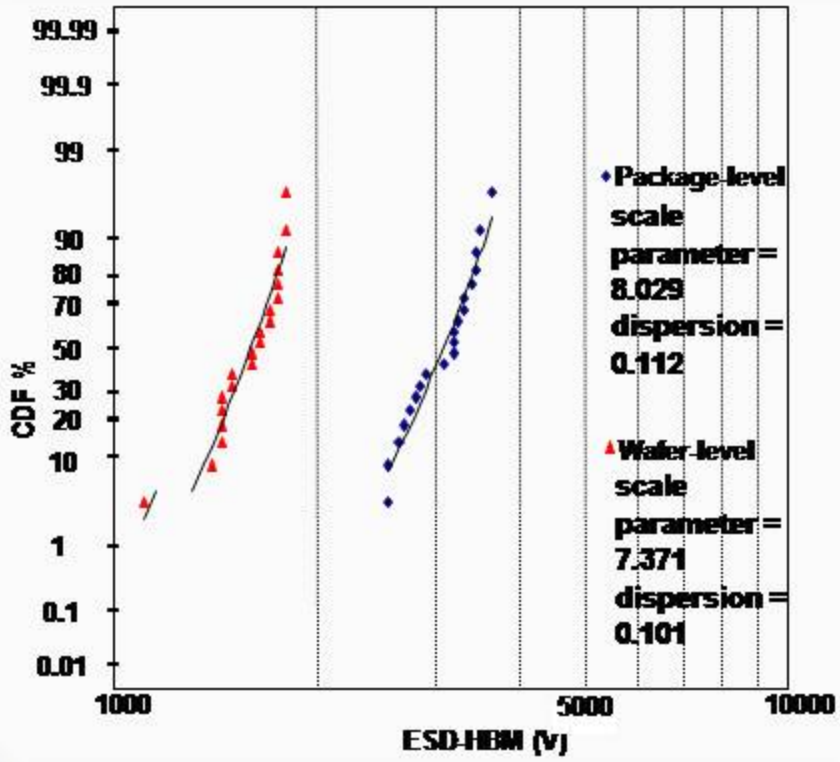


Typical high current I-V curve of a grounded-gate NMOS transistor as the ESD protection structure for the 0.25um technology as an example.

HBM Correlations

Good HBM correlations between wafer level testing and package level testing

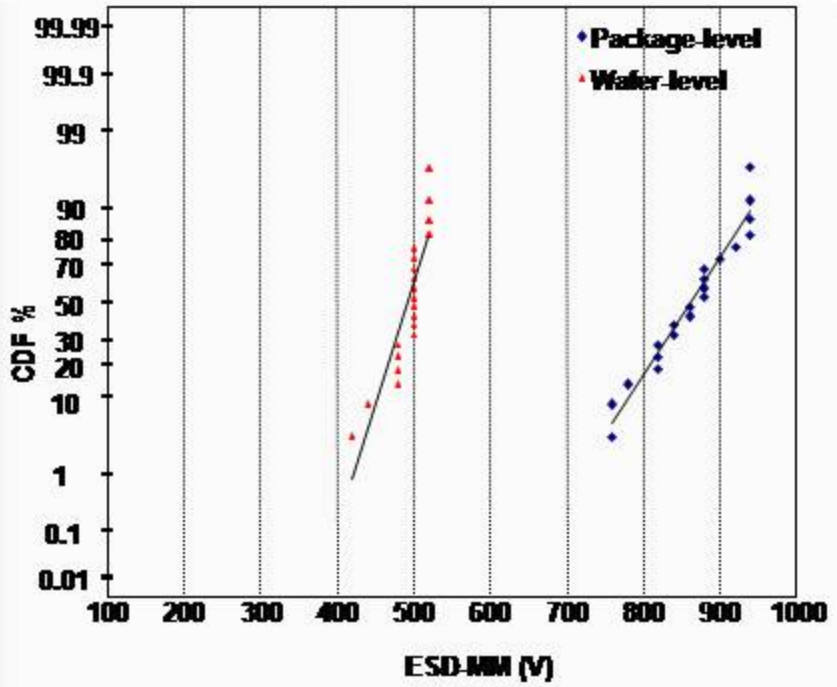


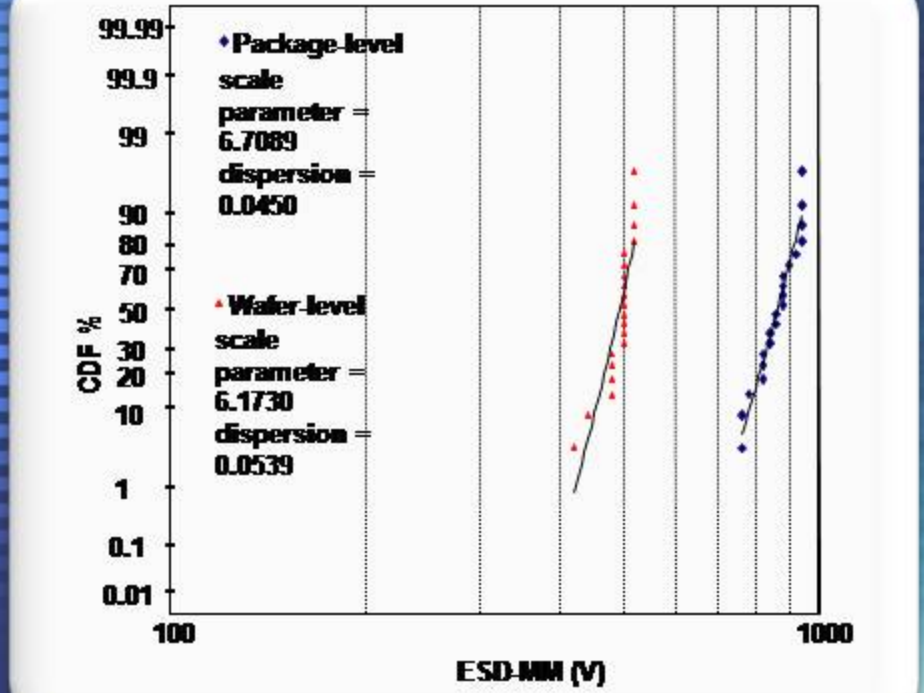


CDF of HBM measured through wafer-level and package-level tests on (a) normal plot and (b) lognormal plot, in which the grounded gate NMOS transistor (W/L = 280um/1.6um) is used as the ESD protection structure for the 0.25um technology.

MM Correlations

Good HBM correlations between wafer level testing and package level testing





CDF of MM measured through wafer-level and package-level tests on (a) normal plot and (b) lognormal plot, in which the grounded gate NMOS transistor (W/L = 200/0.5um) is used as the ESD protection structure for the 0.15um technology.

ESD Miscorrelations

Good correlations between HBM and TLP for non-silicide devices

Bad correlations between HBM and TLP for silicide devices

Circuit A: NMOS with inverter driver

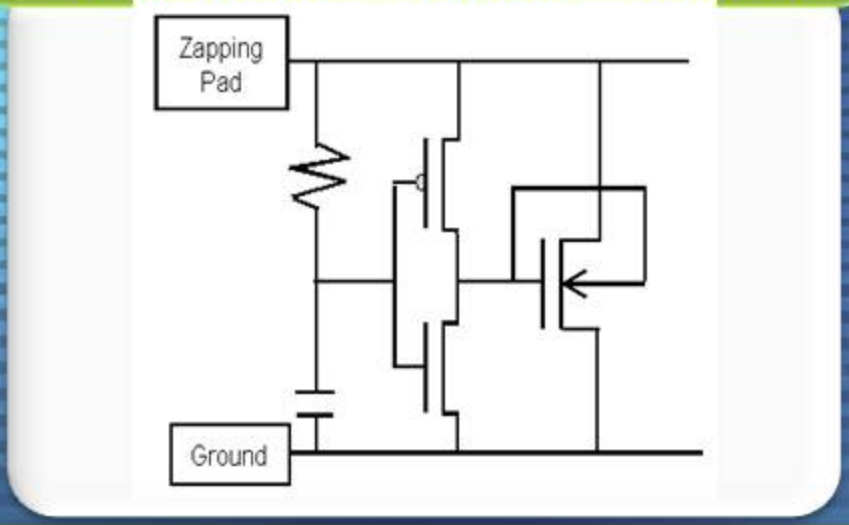
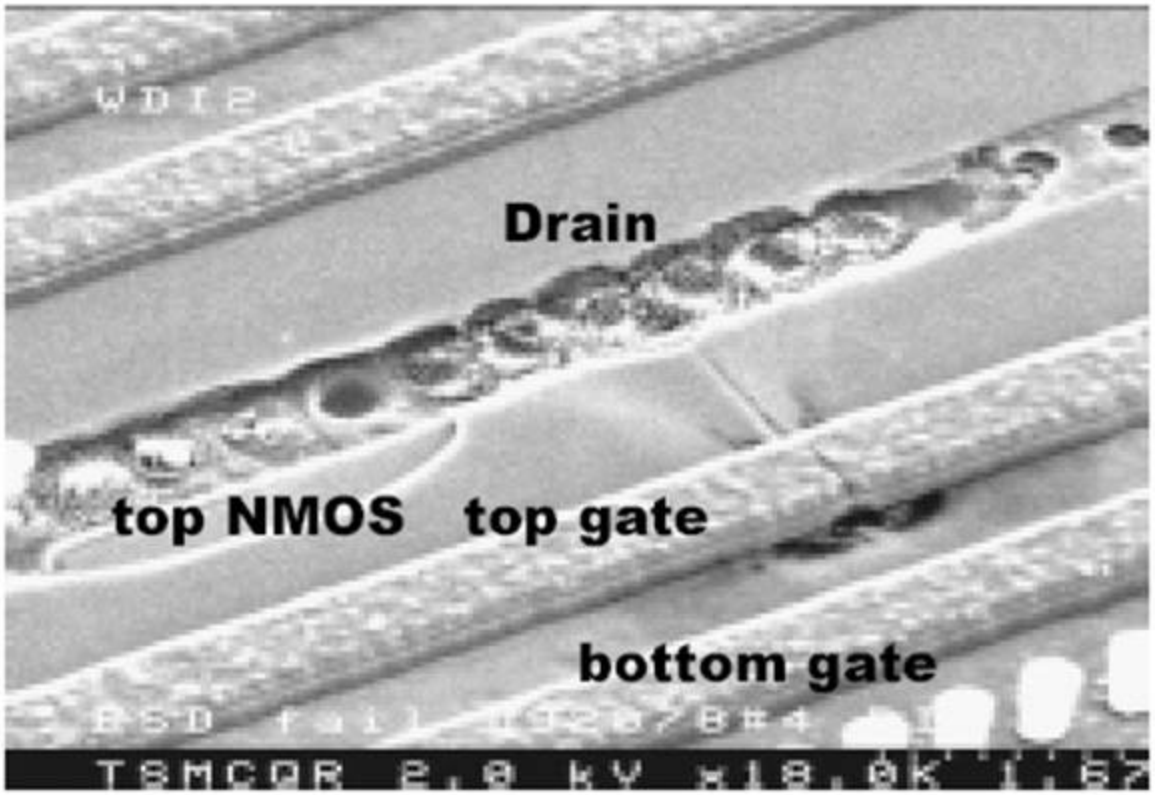


Table 1: ESD results for circuit A

ESD immunity	It2(A)	HBM(kV)	V-HBM/(1.5kohm x It2)	MM(V)
non-silicide, l=0.4µm	3.52	5.7	1.08	475
silicide, l=0.4µm	3.15	0.75	0.16	50
silicide, l=1µm	3.31	1.15	0.23	50
silicide, l=1.5µm	3.03	3.2	0.70	100

Failure Analysis for ESD

Figure out where the product weak point is.

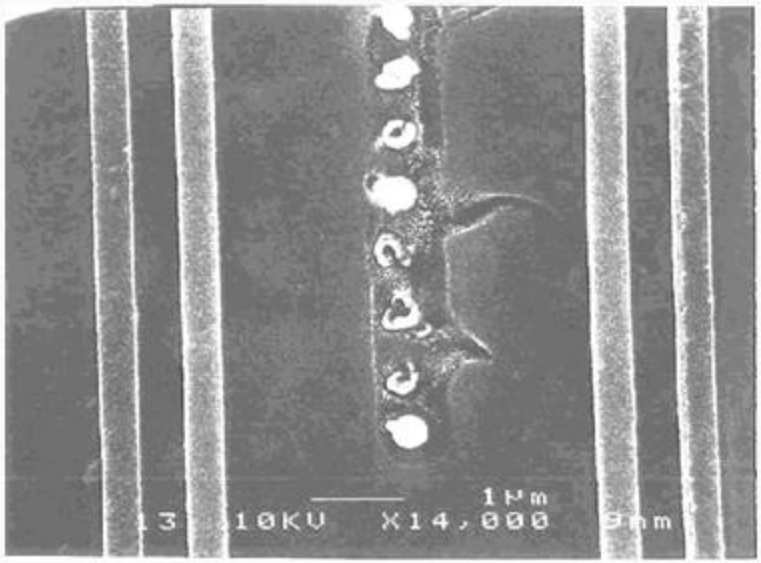


Filament formation is from the drain to source of top NMOS.

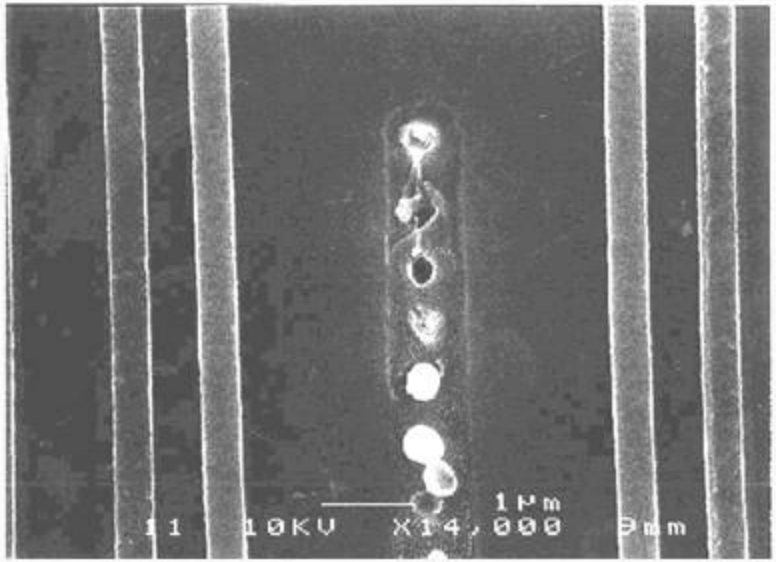
Failure Analysis for ESD

Comprehend why different ESD robustness happen on distinct devices

PESD



Failure analysis – without PESD



Failure analysis – with PESD

Failure Analysis Pictures

Fig.4. SEM photograph showing holes at the silicon-to-LOCOS interface in the drain diffusion of an input protection. This is a top view taken after partial oxide etching.

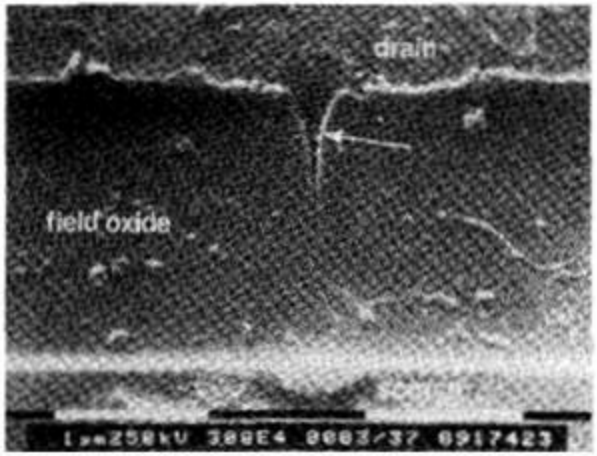


Fig.5. SEM photograph of the top view of an input protection circuit showing filamentation damage between adjacent n diffusion regions under the field oxide. The photograph was made after field oxide etch.

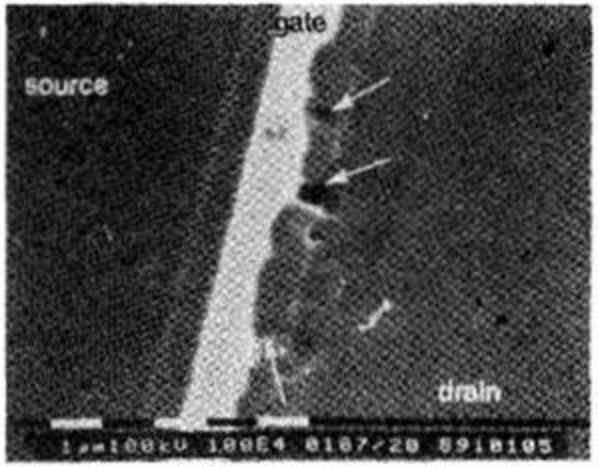


Fig.6. SEM photograph of an NMOS transistor, after partial n^+ polysilicon etch to expose the gate oxide, showing gate-oxide damage.

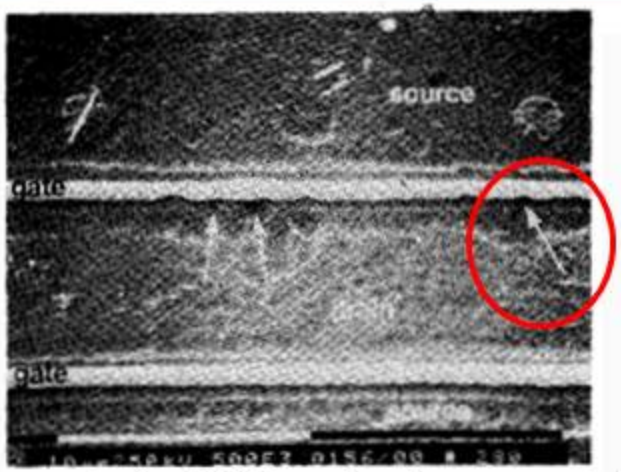


Fig.7. SEM photograph of an NMOS transistor in an output buffer, after partial n^+ polysilicon etch, showing drain/polysilicon edge damage. (notching).

Failure Analysis Pictures

Fig.8. SEM photograph of a contact hole in the drain diffusion region of an NMOST output transistor showing a hole due to contact spiking.

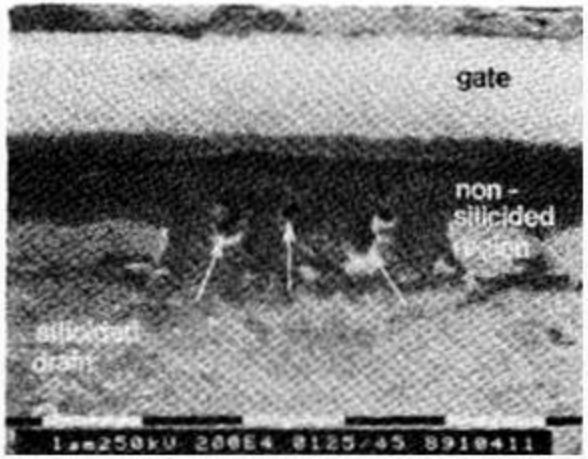


Fig.9. SEM photograph of an NMOS output transistor using the silicide blocking mask. The melt region is seen in the area between the silicide edge and the polysilicon edge.

Conclusion

The same ESD pass voltages occur along the IC size scales down.

- HBM pass voltage is the same. (if no environment change)
- MM pass voltage is the same. (if no environment change)

Big challenges in ESD protection

Solving ESD issues from the full view

- ESD design
- ESD related process
- ESD test
- ESD failure analysis

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Thanks a lot for your attention!